Product Specification 1000.694201 27 July 2021 16:30:08 Issue Date

Icemos Technology Ltd

Customer

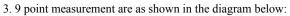
Part Number

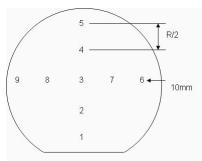
Category	Parameter		Specification	Measurement Method
OverallWafer	1.0	Diameter	100.00 +/- 0.50 mm	
	2.0	Primary Flat Orientation	{110} +/- 1 degree	Wafer Vendor
	3.0	Primary Flat Length	32.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	none/semi std	
	5.0	Overall Thickness	480.00 +/- 26.00 μm	ADE 100%
	6.0	Total Thickness Variation (TTV)	<5.00μm	Guaranteed by Process
	7.0	Bow	<60.00μm	ADE to ASTM F534, 20%
	8.0	Warp	<60.00μm	ADE to ASTM F657, 20%
	9.0	Edge Chips	0	Bright Light, 100% (note 2)
	10.0	Edge Exclusion	5mm	
HandleSilicon	11.0	Handle Growth Method	CZ	Wafer Vendor - Topsil only
	12.0	Handle Orientation	{100} +/- 0.5 degree	Wafer Vendor
	13.0	Handle Thickness	450.00 +/- 25.00 μm	ADE, 100%
	14.0	Handle Doping Type	P	Wafer Vendor
	15.0	Handle Dopant	Boron	Wafer Vendor
	16.0	Handle Resistivity	<0.01 Ohmcm	Wafer Vendor
	17.0	Backside Finish	Lapped and etched with lasermark.	Wafer Vendor
DeviceSilicon	18.0	Device Growth Method	CZ	Wafer Vendor - Topsil only
	19.0	Device Orientation	{100} +/- 0.5 degree	Wafer Vendor
	20.0	Nominal Thickness	30.00 +/- 1.00 μm	ADE single Point
	21.0	Distance to device silicon edge from wafer edge	< 2 mm	Guaranteed by Process
	22.0	Device Doping Type	P	Wafer Vendor
	23.0	Device Dopant	Boron	Wafer Vendor
	24.0	Device Resistivity	1~30 Ohm-cm	Wafer Vendor
	25.0	Voids	0	Bright Light, 100% (note 2)
	26.0	Scratches	0	Bright Light, 100% (note 2)
	27.0	Haze	none	Bright Light, 100% (note 2)

Page 1 of 2 27/01/2022 www.icemostech.com

Part Number		Customer	
Category	Parameter	Specification	Measurement Method
Shipping Details	Wafer per box :	Max 25	
	Packaging:	Taped Polypropylene Wafer Box Empak, Ultrapak, 100.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	
Explanatory Notes	1. Microscope inspec	ction performed using microscope scan as below. 5x objective.	
	2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall		

2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overal Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.





Additional Information