Part Number	Customer

Category		Parameter	Specification	Measurement Method
OverallWafer	1.0	Diameter	200.00 +/- 0.20 mm	
	2.0	Notch Direction	{110}+/-1.0 degree	Wafer Vendor
	3.0	Notch or Flat	Notch	Wafer Vendor
	4.0	Notch Depth Tolerance	1mm, -1mm / + 0.25mm	Wafer vendor
	5.0	Notch Angle	90 deg, tolerance -1deg to +5deg (89deg ~ 95deg).	Wafer vendor
	6.0	Overall Thickness	716.00 +/- 15.55 µm	ADE, 100%
	7.0	Total Thickness Variation (TTV)	<2.50µm	Guaranteed by Process. Target <2.5um TTV. Best Effort for Qualification lot.
	8.0	Wafer Flatness (SFPD)	<0.35um. 60 Sites, 22X22mm. Partials included.	ADE. Best Effort for Qualification lot.
	9.0	Bow	<80.00µm	ADE to ASTM F534, 100%
	10.0	Warp	<80.00µm	
	11.0	Frontsurface condition	Polished	
	12.0	Edge Chips	0	Bright Light, 100% (note 2)
	13.0	Edge Exclusion	5mm	
	14.0	Silicon Dislocation Etch Pit Density	OISF <100 per cm2. 1100deg, 2hr thermal cycle.	Wafer vendor
	15.0	Lasermarking	Backside, opposite to notch.	According to STM general specification 063888
HandleSilicon	16.0	Handle Growth Method	CZ/MCZ	Wafer Vendor
	17.0	Handle Orientation	{100} +/- 0.5 degree	Wafer Vendor
	18.0	Handle Thickness	650.00 +/- 15.00 µm	ADE, 100%
	19.0	Handle Doping Type	P	Wafer Vendor
	20.0	Handle Dopant	Boron	Wafer Vendor
	21.0	Handle Resistivity	2 ~ 10 Ohmcm	Wafer Vendor
	22.0	Handle Oxygen Concentration	<16 ppma	ASTM F1180 new
	23.0	Handle Carbon Concentration	<0.3 ppma new ASTM F1391	Wafer vendor
	24.0	Resistivity variation (within wafer)	<20%	Wafer vendor
	25.0	Backside Finish	Polished with lasermark and 1um oxide.	Guaranteed by process
BuriedOxide	26.0	Oxide Type	Thermal	
	27.0	Oxide Thickness	10,000.00 +/- 500.00 A	9 Point Measurement. Nanospec centre point, 4%
	28.0	Oxide formed on	Handle wafer	
DeviceSilicon	29.0	Device Growth Method	CZ/MCZ	Wafer Vendor
	30.0	Device Orientation	{100} +/- 0.5 degree	Wafer Vendor
	31.0	Nominal Thickness	65.00 +/- 0.50 µm	FTIR, 100% 9-Pt (note3)

Part Number	Customer

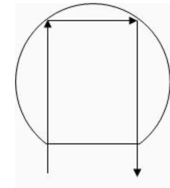
Category		Parameter	Specification	Measurement Method
DeviceSilicon	32.0	Distance to device silicon edge from wafer edge	<= 2mm	Typical by Process
	33.0	Edge Removal Depth in Handle	<100um	Process performance guarantee + SEM/profilometer.
	34.0	Edge Removal Angle	<90 degrees	Guaranteed by process
	35.0	Device Doping Type	P	Wafer Vendor
	36.0	Device Dopant	Boron	Wafer Vendor
	37.0	Device Resistivity	2 ~ 10 Ohmcm	Wafer Vendor
	38.0	Oxygen Concentration	<13 ppma	ASTM F1180 new
	39.0	Carbon Concentration	<0.3 ppma new ASTM F1391	Wafer vendor
	40.0	Resisitivity variation (within wafer)	<11%	Wafer vendor
	41.0	Voids	None >500um diameter.	Bright Light, 100% (note 2)
	42.0	Scratches	0	Bright Light, 100% (note 2)
	43.0	Haze	None	Bright Light, 100% (note 2)

Part Number	Customer

Category	Parameter	Specification	Measurement Method
Shipping Details	Wafer per box :	Max 25	
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 200.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	

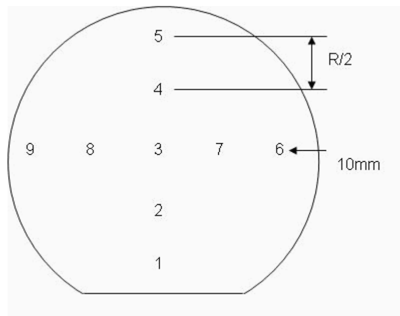
Explanatory Notes

1. Microscope inspection performed using microscope scan as below. 5x objective.



2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information