IceMOS Technology

TSV Solutions

Applications

Our customised Through Silicon Via solutions are used in the following fields:

- SOI solutions for MEMS/MST
- Microfluidics/flow sensors
- RF MEMS
- Optoelectronics
- Smart Power
- Advanced Analog ICs

End Markets:

- Telecommunications
- Medical
- Automotive
- Consumer
- Instrumentation

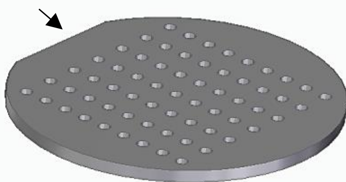
IceMOS Technology have developed an innovative and powerful through-wafer interconnect technology which can allow device designers in both standard IC and MEMS device industries overcome packaging problems associated with their designs. Using this interconnect solution allows many of our customers to migrate their designs easily to a wafer level package with solder bumped contacts.

The IceMOS Technology solution is a pre-processed substrate which is delivered to the customer with the interconnect already formed within the substrate. This substrate is fully CMOS compatible.

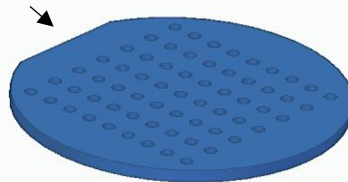
All interconnect is performed using through wafer etching and refill and heavily doped polysilicon. The wafers meet all standard specifications for surface metallic contamination, planarity and particle count. We have verified stable substrate performance up to diffusion temperatures of 1200C.

IceMOS will develop customer specific through-wafer interconnect solution in partner, taking the preferred interconnect pattern and implementing it on the wafer for easy connectivity to a circuit or sensor. The TSV may be beside or below existing bond pads. The design is optimised and fully customised to the customer's requirements.

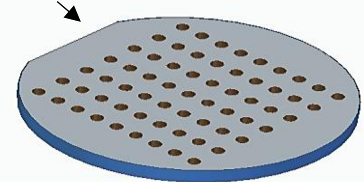
TSV Wafer



TSV Wafer with Liner Oxide



TSV Wafer with Polysilicon



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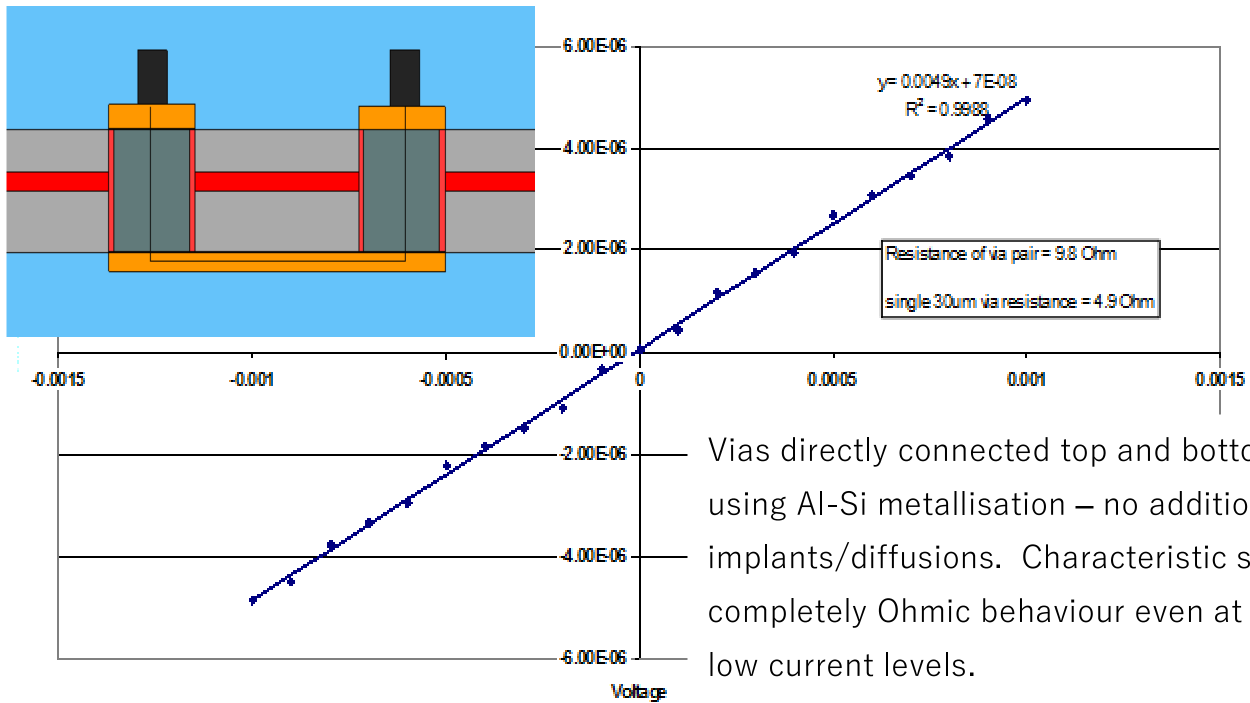

Vias directly connected top and bottom using Al-Si metallisation – no additional implants/diffusions. Characteristic shows completely Ohmic behaviour even at very low current levels.

TSV Specification

Parameter	Specification Range
Aspect Ratio of Via	<15:1
Wafer Diameter	100mm & 150mm
Wafer Thickness	300–525µm
Max. Diameter	40µm on smallest side
Min. Pitch	90µm (3x via width)
Poly Resistivity	<5 mΩ-cm
Isolation Resistance	Determined by oxide liner (design dependent)
Oxide Liner Thickness	0.2–2µm

The above is a standard IceMOS specification; however, we are always happy to work with our customers to engineer specific solutions. If you would like to discuss an alternative specification, please contact our sales team: sales@icemostech.com

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