Icemos Technology Ltd **Product Specification** **1000.526101** Issue Date 24 January 2018 15:3

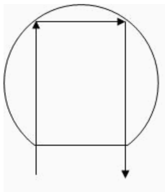
Part Number Customer

Category		Parameter	Specification	Measurement Method
OverallWafer	1.0	Diameter	150.00 +/- 0.50 mm	
	2.0	Primary Flat Orientation	{110}+/-1.0 degree	Wafer Vendor
	3.0	Primary Flat Length	57.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	None	
	5.0	Secondary Flat Length	None	Wafer Vendor
	6.0	Overall Thickness	335.00 +/- 11.00 µm	ADE, 100%
	7.0	Total Thickness Variation (TTV)	<5.00µm	Guaranteed by Process
	8.0	Bow	<60.00µm	ADE to ASTM F534, 20%
	9.0	Warp	<60.00µm	ADE to ASTM F657, 20%
	10.0	Edge Chips	0	Bright Light, 100% (note 2)
	11.0	Edge Exclusion	5mm	
HandleSilicon	12.0	Handle Growth Method	CZ	Wafer Vendor
	13.0	Handle Orientation	{100} +/- 1.0 degree	Wafer Vendor
	14.0	Handle Thickness	300.00 +/- 10.00 µm	ADE, 100%
	15.0	Handle Doping Type	P	Wafer Vendor
	16.0	Handle Dopant	Boron	Wafer Vendor
	17.0	Handle Resistivity	0.005 ~ 0.01 Ohmcm	Wafer Vendor
	18.0	Backside Finish	Polished with lasermarking.	Process conditions
BuriedOxide	19.0	Oxide Type	NONE	
DeviceSilicon	20.0	Device Growth Method	FZ	Wafer Vendor
	21.0	Device Orientation	{100} +/- 1.0 degree	Wafer Vendor
	22.0	Nominal Thickness	35.00 +/- 1.00 µm	ADE single point - 100%
	23.0	Distance to device silicon edge from wafer edge	<= 2.0mm	Guaranteed by process
	24.0	Device Doping Type	P	Wafer Vendor
	25.0	Device Dopant	Boron	Wafer Vendor
	26.0	Device Resistivity	>1000 Ohmcm	Wafer Vendor
	27.0	Voids	0	Bright Light, 100% (note 2)
	28.0	Scratches	0	Bright Light, 100% (note 2)
	29.0	Haze	none	Bright Light, 100% (note 2)

Category	**Parameter**	**Specification**	**Measurement Method**
Shipping Details	Wafer per box :	Max 25	
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 150.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	

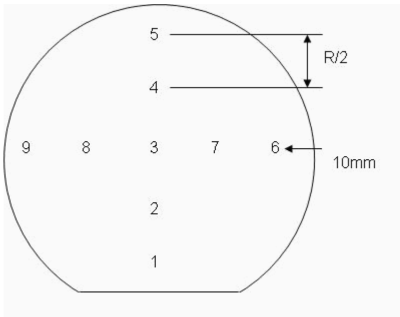
Explanatory Notes

1. Microscope inspection performed using microscope scan as below. 5x objective.



2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information