Icemos Technology Ltd Product Specification 1003.007605 Issue Date 28 February 2011 14:0

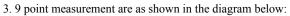
Part Number	Customer	

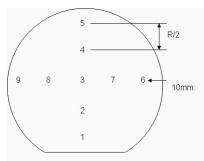
Category		Parameter	Specification	Measurement Method	
OverallWafer	1.0	Diameter	100.00 +/- 0.50 mm		
	2.0	Primary Flat Orientation	{110}+/-1 degree	Wafer Vendor	
	3.0	Primary Flat Length	32.50 +/- 2.50 mm	Wafer Vendor	
	4.0	Secondary Flat Orientation	none / semi std	wafer vendor	
	5.0	Overall Thickness	525.00 +/- 25.00 μm	ADE, 100%	
	6.0	Total Thickness Variation (TTV)	<10.00um	ADE, 100% measurement	
	7.0	Bow	<40.00μm	ADE to ASTM F534, 20%	
	8.0	Warp	<40.00μm	ADE to ASTM F657, 20%	
	9.0	Edge Chips	0	Bright Light, 100% (note 2)	
	10.0	Edge Exclusion	5mm		
HandleSilicon	11.0	Handle Growth Method	FZ	Wafer Vendor	
	12.0	Handle Orientation	{100} +/- 1 degree	Wafer Vendor	
	13.0	Handle Thickness	525.00 +/- 25.00 μm	ADE, 100%	
	14.0	Handle Doping Type	N	Wafer Vendor	
	15.0	Handle Dopant	Phosphorous	Wafer Vendor	
	16.0	Handle Resistivity	> 1000 Ohmcm	Wafer Vendor	
	17.0	Backside Finish	Polished with 1.8um +/- 0.2um oxide and lasermark, no polysilicon. Planarise after phosphorous deposition of poly	Wafer Vendor	
DeviceSilicon	18.0	LPD Count	<30.00pces	@0.3um, Tencor 6220 particle counter	
	19.0	Scratches	0	Bright Light, 100% (note 2)	
	20.0	Haze	none	Bright Light, 100% (note 2)	
	21.0	Surface	front side prime polished (before oxide and poly deposition)	Guaranteed by process	
	23.0	Device Field Oxidation	20,000.00 +/- 1,000.00 A	Nanospec 4%, 5pt	
Trench	24.0	Poly refill thickness	20000A +/- 1000A, doped as per the schedule in notes. Sheet resistance of poly <2.8 Ohms per sq	4 pt probe 100%	

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Part Number		Customer		
Category	Parameter	Specification		Measurement Method
Shipping Details	Wafer per box :	Max 25		
	Packaging:	Taped Polypropylene Wafer Box Empak, Ultrapak, 100.00mm Antistatic Double Bagging		
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness		
Explanatory Notes	1. Microscope inspec	tion performed using microscope scan a	s below. 5x objective	e.
	2. All bright light ins	pections performed exclude all wafer are	ea outside the edge e	exclusion defined in Overall

2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overal Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.





Additional Information