Icemos Technology Ltd Product Specification 1000.312101 Issue Date 08 August 2012 11:46

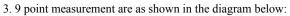
D M 1	O 4	
Part Number	Customer	

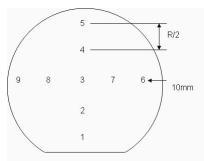
Category		Parameter	Specification	Measurement Method
OverallWafer	1.0	Diameter	100.00 +/- 0.50 mm	WaferVendor
	2.0	Primary Flat Orientation	<110> +/- 1 degree	Wafer Vendor
	3.0	Primary Flat Length	32.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	none	Wafer Vendor
	5.0	Overall Thickness	970.00 +/- 7.00 um	Guaranteed by Process
	6.0	Total Thickness Variation (TTV)	<5.00um	Guaranteed by Process
	7.0	Bow	<40.00um	Guaranteed by Process
	8.0	Warp	<40.00um	Guaranteed by Process
	9.0	Edge Exclusion	5 mm	Guaranteed by Process
HandleSilicon	10.0	Handle Growth Method	CZ	Wafer Vendor
	11.0	Handle Orientation	<111> off 2.5 - 3.5deg	Wafer Vendor
	12.0	Handle Thickness	670.00 +/- 5.00 um	Guaranteed by Process
	13.0	Handle Doping Type	P	Wafer Vendor
	14.0	Handle Dopant	Boron	Wafer Vendor
	15.0	Handle Resistivity	< 0.005	Wafer Vendor
	16.0	Backside Finish	Lapped and etched with no oxide and lasermark	Wafer Vendor
DeviceSilicon	17.0	Device Growth Method	FZ	Wafer Vendor
	18.0	Device Orientation	<111> +/- 1 degree	Wafer Vendor
	19.0	Nominal Thickness	300.00 +/- 2.00 um	Guaranteed by Process, ADE single point, 100%
	20.0	Distance to device silicon edge from wafer edge	<= 2mm	Guaranteed by Process
	21.0	Device Doping Type	P	Guaranteed by Process
	22.0	Device Dopant	Boron	Guaranteed by Process
	23.0	Device Resistivity	12000 - 20000 Ohmem	Wafer Vendor
	24.0	Voids	none	Guaranteed by Process, SAM inspection
	25.0	Haze	none	Guaranteed by Process, Bright LIght inspection
	26.0	Scratches	none	Guaranteed by Process, Bright LIght inspection

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Part Number		Customer	
Category	Parameter	Specification	Measurement Method
Shipping Details	Wafer per box :	Max 25	
	Packaging:	Taped Polypropylene Wafer Box Empak, Ultrapak, 100.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	
Explanatory Notes	1. Microscope inspec	tion performed using microscope scan as below. 5x objective.	
		pections performed exclude all wafer area outside the edge exclusio	on defined in Overall

Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.





Additional Information