Part Number	Customer

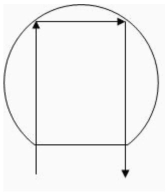
Category		**Parameter**	**Specification**	**Measurement Method**
OverallWafer	1.0	Diameter	100.00 +/- 0.50 mm	WaferVendor
	2.0	Primary Flat Orientation	<110> +/- 1 degree	Wafer Vendor
	3.0	Primary Flat Length	32.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	none/SEMI	Wafer Vendor
	5.0	Overall Thickness	400.00 +/- 5.00 um	Guaranteed by Process
	6.0	Total Thickness Variation (TTV)	<5.00um	Guaranteed by Process
	7.0	Bow	<40.00um	Guaranteed by Process
	8.0	Warp	<40.00um	Guaranteed by Process
	9.0	Edge Exclusion	5 mm	Guaranteed by Process
HandleSilicon	10.0	Handle Growth Method	CZ	Wafer Vendor
	11.0	Handle Orientation	<100> +/- 0.5 degree	Wafer Vendor
	12.0	Handle Thickness	385.00 +/- 5.00 um	Guaranteed by Process
	13.0	Handle Doping Type	N	Wafer Vendor
	14.0	Handle Dopant	Arsenic	Wafer Vendor
	15.0	Handle Resistivity	< 0.005	Wafer Vendor
	16.0	Backside Finish	Polished with no oxide and lasermark	Wafer Vendor
DeviceSilicon	17.0	Device Growth Method	FZ	Wafer Vendor
	18.0	Device Orientation	<100> +/- 0.5 degree	Wafer Vendor
	19.0	Nominal Thickness	15.00 +/- 0.50 um	Guaranteed by Process, FTIR 9pt 100%
	20.0	Distance to device silicon edge from wafer edge	<= 2mm	Guaranteed by Process
	21.0	Device Doping Type	N	Guaranteed by Process
	22.0	Device Dopant	Phosphorous	Guaranteed by Process
	23.0	Device Resistivity	400-800 Ohmcm	Wafer Vendor
	24.0	Buried Layer Implant	Energy = 40keV, Dose = 1e14, Species = Phosphorous	Implant Vendor
	25.0	Voids	none	Guaranteed by Process, SAM inspection
	26.0	Haze	none	Guaranteed by Process, Bright LIght inspection
	27.0	Scratches	none	Guaranteed by Process, Bright LIght inspection

Part Number	Customer

Category	**Parameter**	**Specification**	**Measurement Method**
Shipping Details	Wafer per box :	Max 25	
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 100.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	

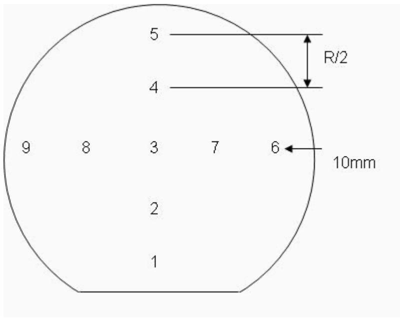
Explanatory Notes

1. Microscope inspection performed using microscope scan as below. 5x objective.



2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information