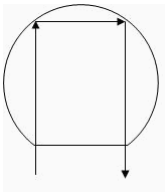
Part Number	Customer

Category		Parameter	Specification	Measurement Method
OverallWafer	1.0	Diameter	100.00 +/- 0.50 mm	
	2.0	Primary Flat Orientation	{110} +/- 1 deg	Wafer Vendor
	3.0	Primary Flat Length	32.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	none	Wafer Vendor
	5.0	Overall Thickness	525.00 +/- 25.00 µm	ADE, 100%
	6.0	Total Thickness Variation (TTV)	<5.00µm	Guaranteed by Process
	7.0	Flatness (SBIR)	<1.50um	ADE 100%
	8.0	Bow	<40.00µm	ADE to ASTM F534, 20%
	9.0	Warp	<40.00µm	ADE to ASTM F657, 20%
	10.0	Edge Chips	0	Bright Light, 100% (note 2)
	11.0	Edge Exclusion	5mm	
HandleSilicon	12.0	Handle Growth Method	CZ	Wafer Vendor
	13.0	Handle Orientation	{111} off 4.0 +/- 0.5 degree	Wafer Vendor
	14.0	Handle Thickness	175.00 +/- 5.00 µm	ADE, 100%
	15.0	Handle Doping Type	N	Wafer Vendor
	16.0	Handle Dopant	Arsenic	Wafer Vendor
	17.0	Handle Resistivity	0.001 - 0.005 Ohm cm	Wafer Vendor
	18.0	Backside Finish	Polished with no oxide & laser ID marking	Wafer Vendor
DeviceSilicon	19.0	Device Growth Method	FZ	Wafer Vendor
	20.0	Device Orientation	{111} off 3.5 +/- 1 degree	Wafer Vendor
	21.0	Nominal Thickness	350.00 +/- 5.00 µm	FTIR, 100% 9-Pt (note3)
	22.0	Distance to device silicon edge from wafer edge	<= 3mm	Typical by Process
	23.0	Device Doping Type	N	Wafer Vendor
	24.0	Device Dopant	Phosphorous	Wafer Vendor
	25.0	Device Resistivity	> 5000 Ohm-cm	Wafer Vendor
	26.0	Voids	< 1% area	100% CSAM inspection
	27.0	Surface	polished prime	Bright light inspection 100%
	28.0	Scratches	none	Bright Light, 100% (note 2)
	29.0	Haze	none	Bright Light, 100% (note 2)
	30.0	LPD Count	<15.00pces	particles 0.5 -1.0um by Tencor 6220

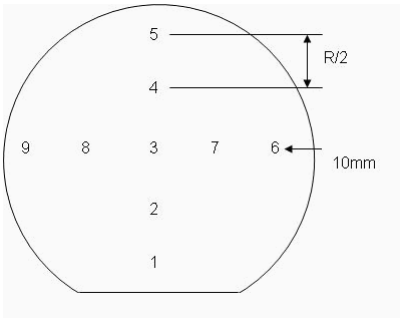
Part Number	Customer

Category	Parameter	Specification	Measurement Method
Shipping Details	Wafer per box :	Max 25	
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 100.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	
Explanatory Notes	1. Microscope inspection performed using microscope scan as below. 5x objective.		



2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information