

Part Number

Customer

Category	Parameter	Specification	Measurement Method
OverallWafer	1.0 Diameter	100.00 +/- 0.50 mm	WaferVendor
	2.0 Primary Flat Orientation	<110> +/- 1 degree	Wafer Vendor
	3.0 Primary Flat Length	32.50 +/- 2.50 mm	Wafer Vendor
	4.0 Secondary Flat Orientation	semi std or none	Wafer Vendor
	5.0 Overall Thickness	762.00 +/- 7.00 um	Guaranteed by Process
	6.0 Total Thickness Variation (TTV)	<5.00um	Guaranteed by Process
	7.0 Bow	<60.00um	ADE to ASTM F534, 20%
	8.0 Warp	<60.00um	ADE to ASTM F657, 20%
	9.0 Edge Chips	0	Bright Light, 100% (note 2)
	10.0 Edge Exclusion	5 mm	Guaranteed by Process
HandleSilicon	11.0 Handle Growth Method	CZ	Wafer Vendor
	12.0 Handle Orientation	<100> +/- 0.5 degree	Wafer Vendor
	13.0 Handle Carbon Concentration	< 5e16 at/cm3	Wafer Vendor
	14.0 Handle Oxygen Concentration	< 1e18 at/cm3	Wafer Vendor
	15.0 Handle Thickness	677.00 +/- 5.00 um	ADE, 100%
	16.0 Handle Doping Type	N	Wafer Vendor
	17.0 Handle Dopant	Arsenic	Wafer Vendor
	18.0 Handle Resistivity	< 0.005	Wafer Vendor
	19.0 Backside Finish	Lapped and etched with no oxide and lasermark	Guaranteed by process
DeviceSilicon	20.0 Device Growth Method	FZ	Wafer Vendor
	21.0 Device Orientation	<100> +/- 0.5 degree	Wafer Vendor
	22.0 Nominal Thickness	85.00 +/- 2.00 um	FTIR, 100% 9pt (note 3). No Offset added to device
	23.0 Distance to device silicon edge from wafer edge	<= 2mm	Typical by Process
	24.0 Device Doping Type	N	Wafer Vendor
	25.0 Device Dopant	Phosphorous	Wafer Vendor
	26.0 Device Resistivity	2800 - 5200 Ohmcm	Wafer Vendor
	27.0 Voids	none	Bright Light, 100% (note 2)
	28.0 Haze	none	Bright Light, 100% (note 2)
	29.0 Scratches	none	Bright Light, 100% (note 2)

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Shipping Details	Wafer per box :	Max 25
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 100.00mm Antistatic Double Bagging
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness



Explanatory Notes 1. Microscope inspection performed using microscope scan as below. 5x objective.

2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information