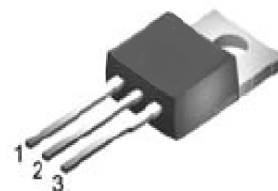
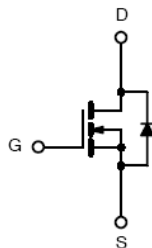


ICE60N150 N-Channel Enhancement Mode MOSFET

Product Summary			
I_D	$T_A=25^\circ\text{C}$	25A	Max
$V_{(BR)DSS}$	$I_D=250\mu\text{A}$	650V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	0.13 Ω	Typ

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High dV/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems



TO220
Standard Metal Heatsink
1=Gate, 2=Drain, 3=Source.

ICEMOS HAS THE LEADERSHIP PATENT PORTFOLIO FOR SUPERJUNCTION MOSFETS (see page 9). ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN, EUROPE.

Maximum Ratings and Thermal Characteristics^b ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	650	V	
Gate-Source Voltage (Static)	V_{GS}	± 20		
Gate-Source Voltage (AC) $f > 1\text{Hz}$	V_{GS}	± 30		
Drain Current	- Continuous ($T_c = 25^\circ\text{C}$)	I_D	25	A
	- Pulsed (limited by T_{jmax})	I_{DM}	82	
Repetitive Avalanche Current (limited by T_{jmax})	I_{AR}	7	A	
Energy in Avalanche (single pulse, $I_D = 3.5\text{A}$)	EAS	690	mJ	
Maximum Power Dissipation ($T_c = 25^\circ\text{C}$)	P_D	208	W	
Operating Junction and Storage Temperature Range	T_J, T_{sg}	-55 to 150	$^\circ\text{C}$	
dV/dt voltage slope ($V_{ds}=480\text{V}, I_D=20\text{A}, T_j = 125^\circ\text{C}$)	dV/dt	50.0	V/ns	
Thermal Resistance ^a	- Junction-to-Ambient	R_{thJA}	62	$^\circ\text{C/W}$
	- Junction-to-Case	R_{thJC}	0.6	

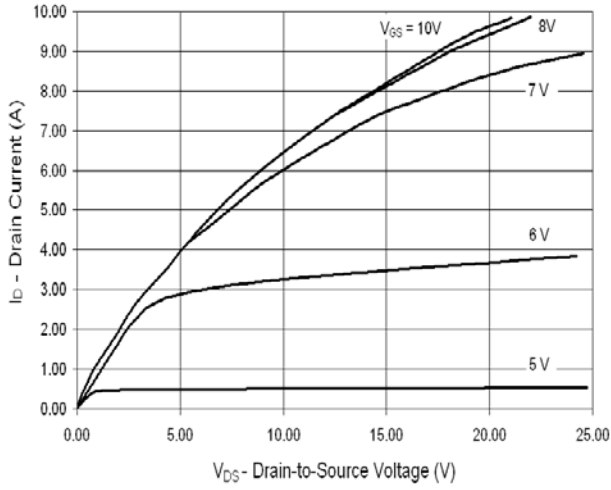
^a When mounted on 1 inch square 2oz copper clad FR-4

^b Preliminary Data Sheet - Specifications subject to change.

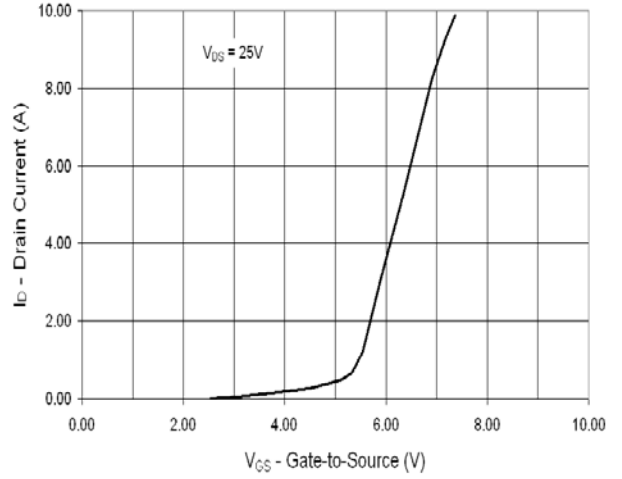
Electrical Characteristics^b (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	650	675		V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =600V, V _{GS} =0V T _J = 150°C		0.1	1	μA
				20	100	μA
I _{GSS}	Gate-Body Leakage	V _{GS} =±20V, V _{DS} =0V		10	100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.5	3	3.5	V
r _{DS(on)}	Drain-to-Source On-State Resistance	V _{GS} =10V, I _D =13A	0.11	0.13	0.15	Ω
		T _J = 150°C	0.33	0.40	0.45	
R _G	Gate Resistance	f = 1MHz	0.2	0.5	0.7	Ω
g _{fs}	Transconductance	V _{DS} > 2*I _D *R _{DS} , I _D = 13A	13	20	30	S
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz	2000	2400	2700	pF
C _{oss}	Output Capacitance		600	780	820	pF
C _{rss}	Reverse Transfer Capacitance		20	50	70	pF
t _{d(on)}	Turn-On Delay Time	V _{GS} =13V, I _D =20A, V _{DS} =380V R _G = 4Ω (External)	5	10	12	nS
t _r	Rise Time		2	5	7	nS
t _{d(off)}	Turn-Off Delay Time		30	67	100	nS
t _f	Fall Time		2	4.5	12	nS
Q _g	Total Gate Charge		V _{GS} =10V, I _D =20A, V _{DS} =480V	65	87	114
Q _{gs}	Gate-to-Source Charge	6		11	13	nC
Q _{gd}	Gate-to-Drain Charge	23		33	36	nC
V _(plateau)	Gate Plateau voltage	2		5.5	7	V
t _{rr}	Source-to-Drain Reverse Recovery Time	I _S =I _F , di/dt=100A/μS, V _{rr} =480V	100	200	250	nS
Q _{rr}	Reverse recovery charge		7	11	14	μC
I _{rm}	Peak reverse recovery current		30	70	80	A
V _{SD}	Diode Forward Voltage	I _S =I _F , V _{GS} =0V	0.5	1.0	1.2	V

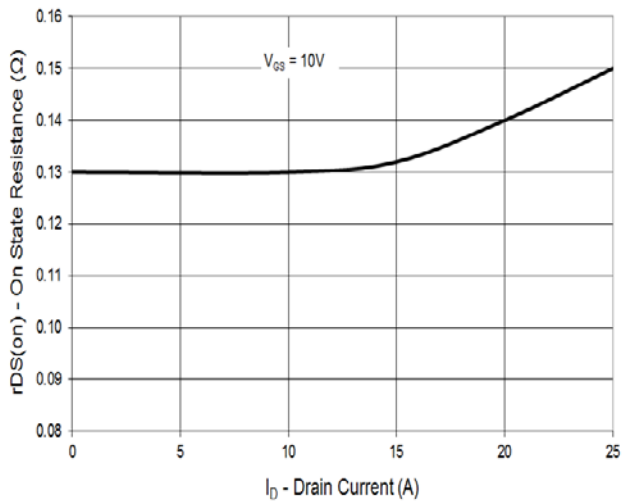
Output Characteristics



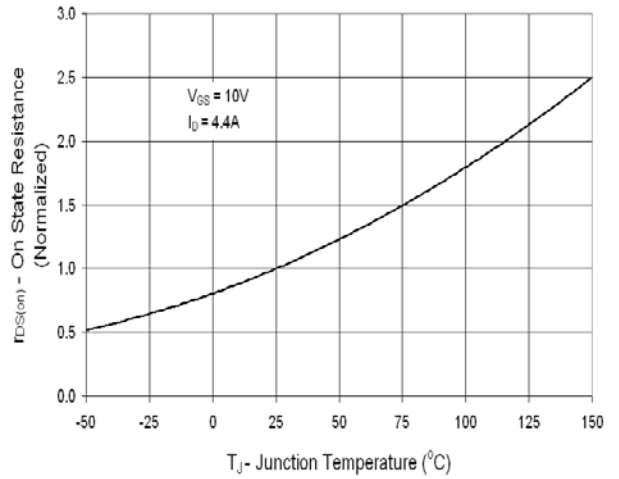
Transfer Characteristics



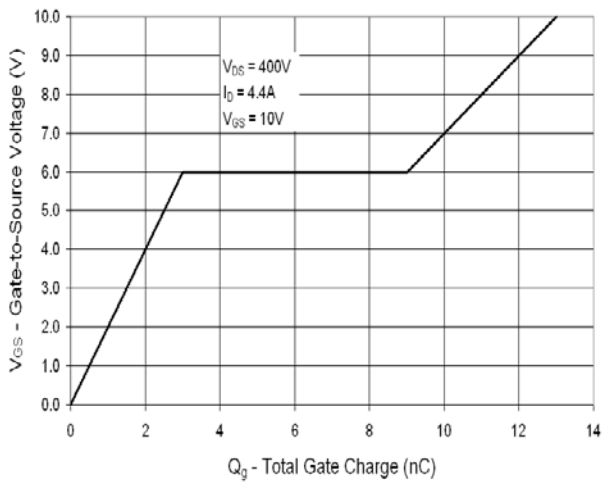
On State Resistance vs. Drain Current



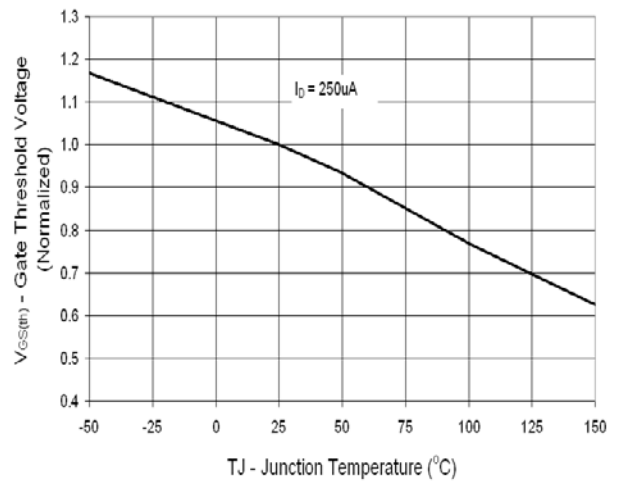
On State Resistance vs. Junction Temperature



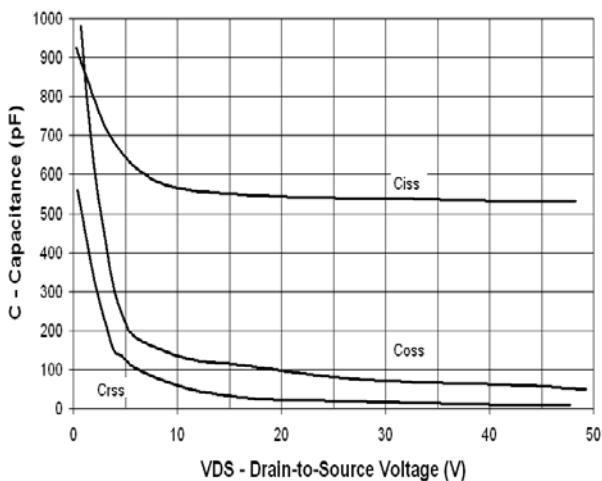
Gate Charge



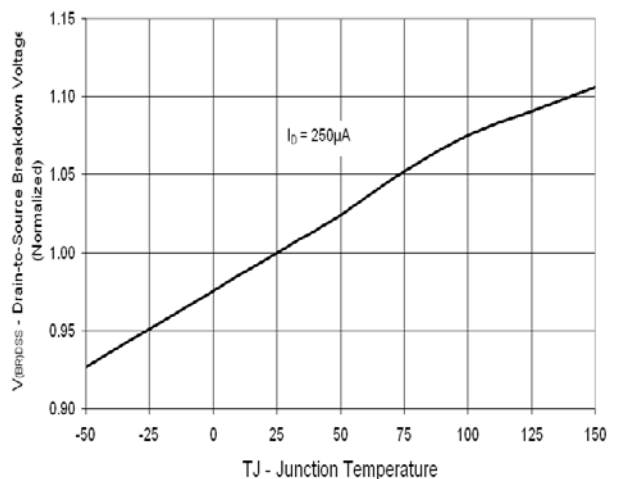
Gate Threshold Voltage vs. Junction Temperature



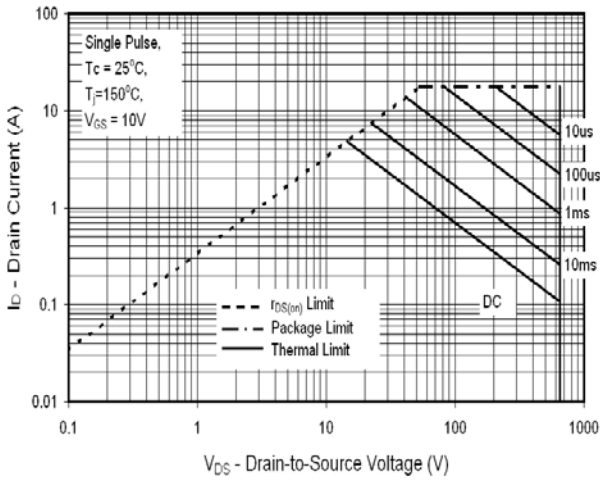
Capacitance



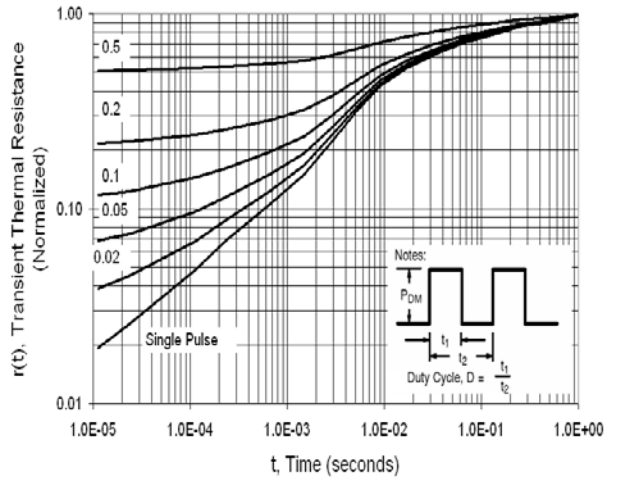
Drain-to-Source Breakdown Voltage vs. TJ

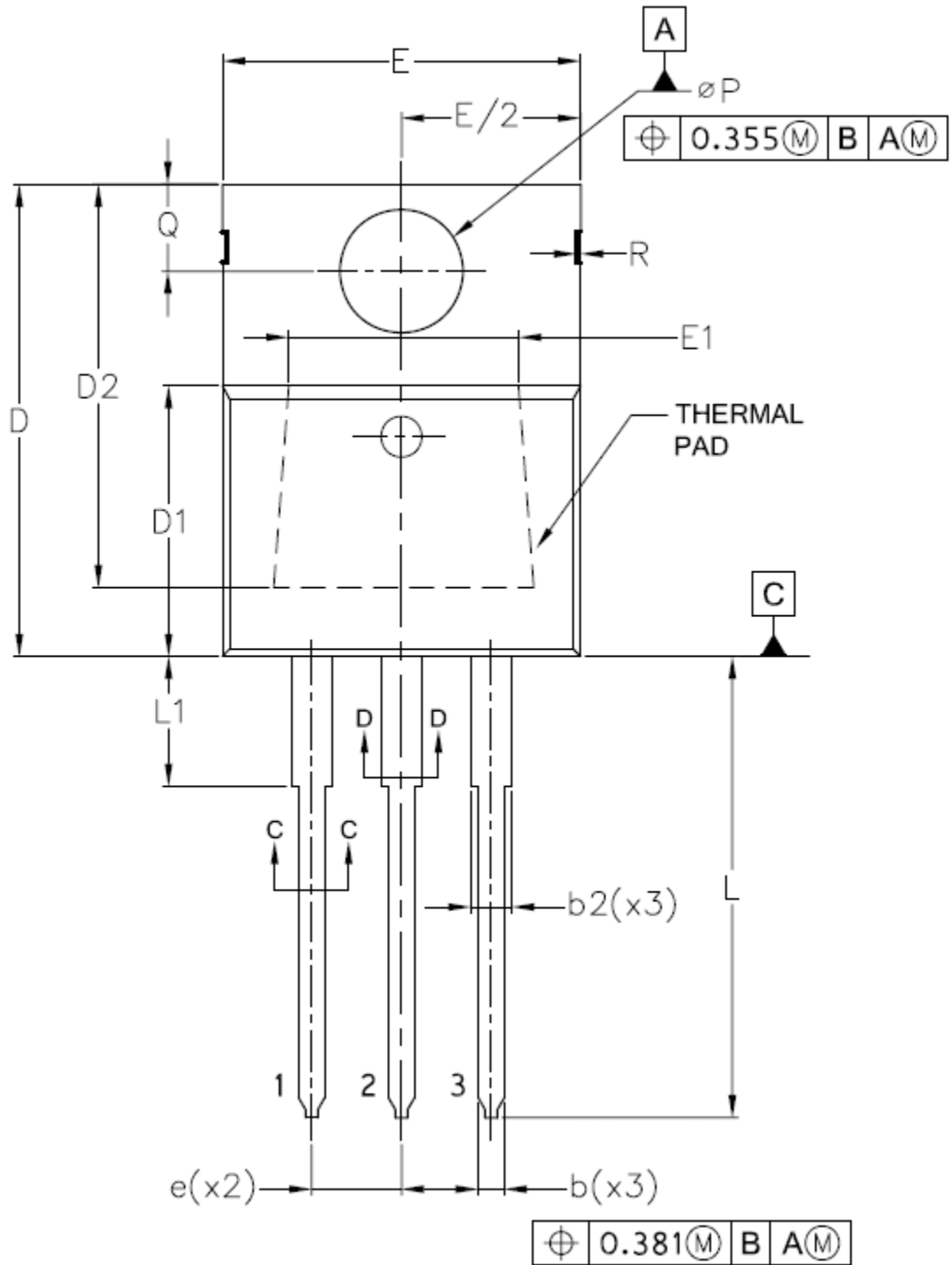


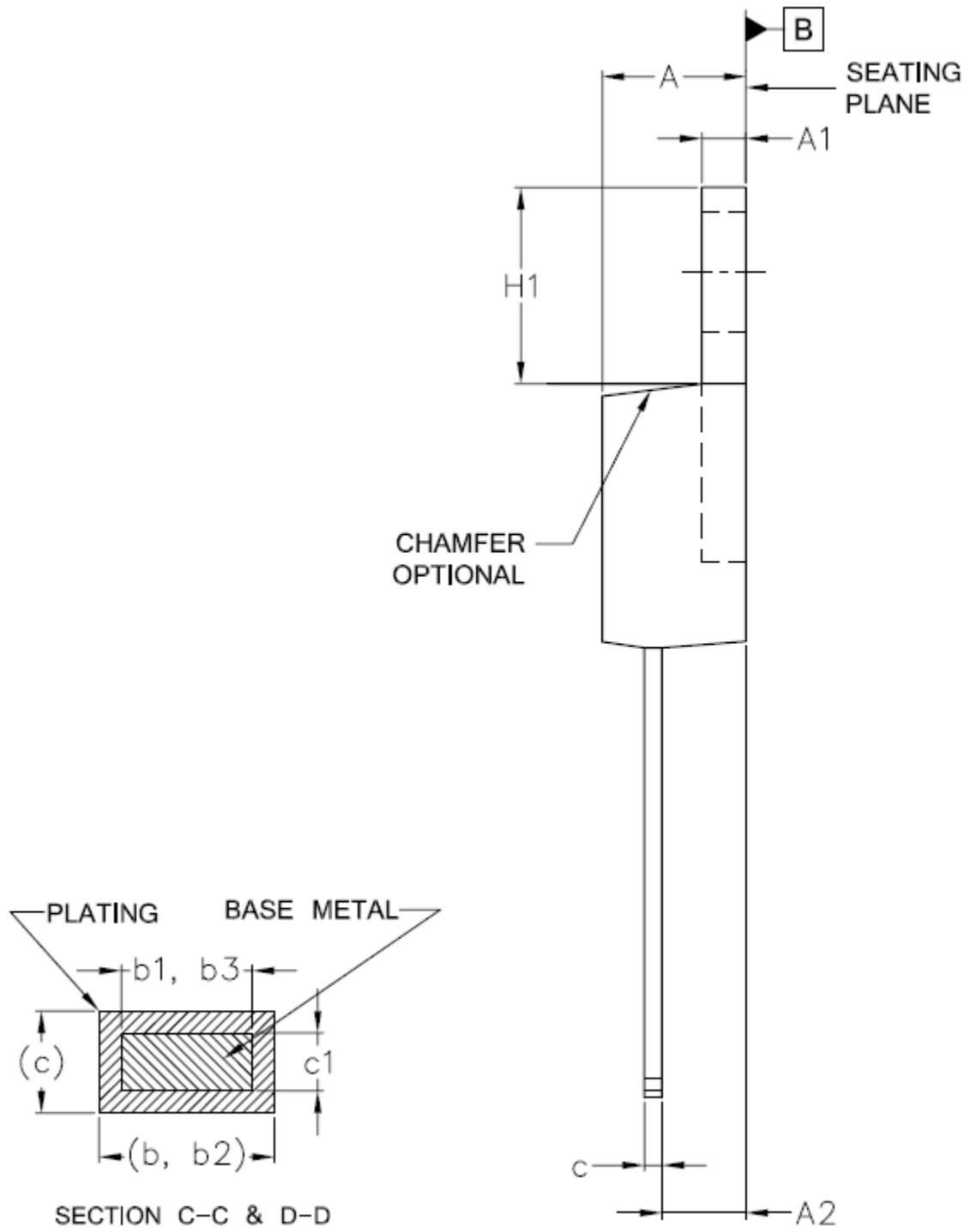
Maximum Rated Forward Biased Safe Operating Area



Transient Thermal Response, Junction-to-Case







SYMBOLS	DIMENSIONS			
	mm		Inch	
	MIN.	MAX.	MIN.	MAX.
A	3.556	4.826	0.140	0.190
A1	0.508	1.397	0.020	0.055
A2	2.032	2.921	0.080	0.115
b	0.381	1.016	0.015	0.040
b1	0.381	0.965	0.015	0.038
c	0.356	0.610	0.014	0.024
c1	0.356	0.559	0.014	0.022
D	14.224	16.510	0.560	0.650
D1	8.382	9.017	0.330	0.355
D2	12.192	12.878	0.480	0.507
E	9.652	10.668	0.380	0.420
E1	6.858	8.890	0.270	0.350
e	2.540 BSC		0.100 BSC	
H1	5.842	6.858	0.230	0.270
L	12.700	14.732	0.500	0.580
∅P	3.810	3.860	0.150	0.151
Q	2.540	3.048	0.100	0.120
b2	1.143	1.778	0.045	0.070
R	1.270 BSC		0.050 BSC	
L1	–	6.350	–	0.250
b3	1.143	1.727	0.045	0.068
f1	3.200 REF.		0.126 REF.	
f2	4.220 REF.		0.166 REF.	
j	1.750 REF.		0.069 REF.	
r	0.510 REF.		0.020 REF.	
N	TO-220-3L			

ICEMOS SUPERJUNCTION PATENT PORTFOLIO

ICEMOS GRANTED PATENTS

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US8,030,133

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US7,364,994

US7,227,197B2

US7,304,944B2

US7,052,982B2

US7,339,252

US7,410,891

US7,439,583

US7,227,197B2

US6,635,906

US6,936,867

US7,015,104

US9,109,110

US7,271,067

US7,354,818

US7,052,982,

US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.