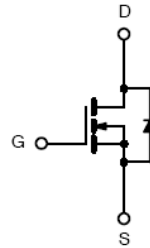
Icemos
Cooler than cool

ICE20N65FP N-Channel Enhancement Mode MOSFET

Product Summary			
I_D	T_A=25°C	20A	Max
$V_{(BR)DSS}$	I_D=250uA	650V	Min
$r_{DS(on)}$	V_{GS}=10V	0.17 Ω	Typ

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High dV/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems



ICEMOS HAS THE LEADERSHIP PATENT PORTFOLIO FOR SUPERJUNCTION MOSFETS (see page 9). ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA,CHINA,KOREA,JAPAN,TAIWAN,EUROPE.

T0220
Full-PAK

Isolated
(T0-220)

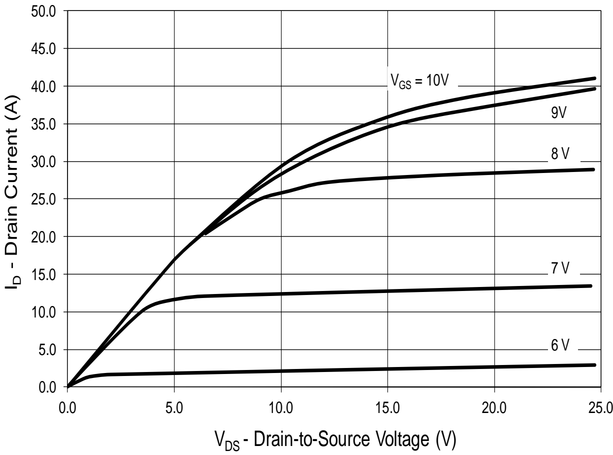
Maximum Ratings and Thermal Characteristics [b] (T_A=25°C unless otherwise noted)

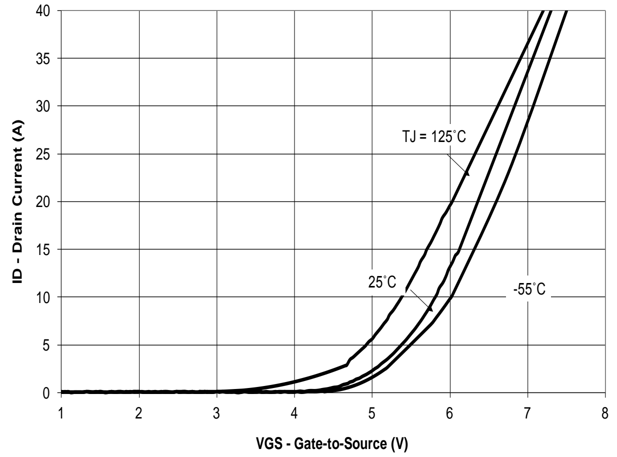
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage (Static)		V_{GS}	±20	
Gate-Source Voltage AC (f > 1Hz)		V_{GS}	±30	
Drain Current	- Continuous (Tc = 25° C)	I_D	20	A
	- Pulsed (limited by Tjmax)	I_{DM}	82	
Repetitive Avalanche Current (limited by Tjmax)		I_{AR}	7	A
Energy in Avalanche (single pulse, ID = 3.5A)		EAS	690	mJ
Maximum Power Dissipation (Tc = 25° C)		P_D	35	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
dV/dt voltage slope (Vds=480V, ID=20A, Tj = 125 °C		dV/dt	50.0	V/ns
Thermal Resistance[a]	- Junction-to-Ambient	R_{thJA}	72	°C/W
	- Junction-to-Case	R_{thJC}	2.50	

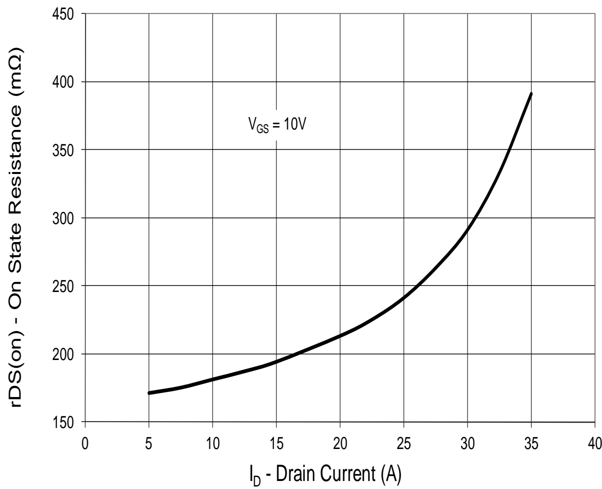
a When mounted on 1 inch square 2oz copper clad FR-4

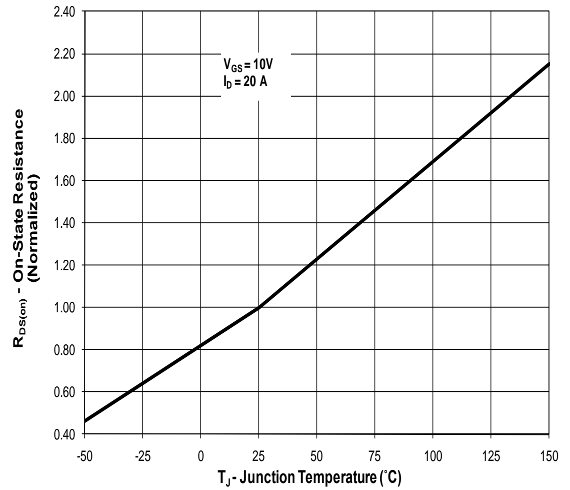
Electrical Characteristics[b] (TJ=25°C unless otherwise specified)

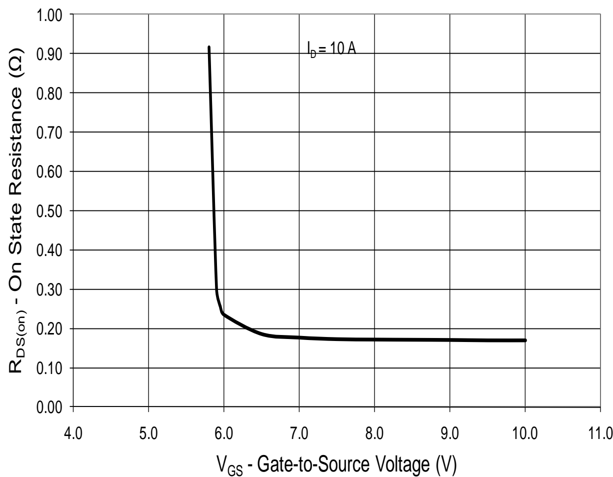
Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	650	675		V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=600V, V_{GS}=0V		0.1	1	μA
		TJ = 150°C		20	100	μA
I_{GSS}	Gate-Body Leakage	V_{GS}=±20V, V_{DS}=0V		10	100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2.5	3	3.5	V
$r_{DS(on)}$	Drain-to-Source On-State Resistance	V_{GS}=10V, I_D=10A	0.139	0.17	0.199	Ω
		TJ = 150°C	0.33	0.40	0.597	
R_G	Gate Resistance	f = 1MHz,	0.2	0.5	0.7	Ω
g_{fs}	Transconductance	V_{DS}> 2*I_D*R_{DS} , I_D = 10A	13	20	30	S
C_{iss}	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MH_Z	900	2400	2700	pF
C_{oss}	Output Capacitance		600	780	820	pF
C_{rss}	Reverse Transfer Capacitance		20	50	70	pF
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=10V, I_D=20A, V_{DS}=380V R_G = 4Ω (External)	5	10	12	nS
t_r	Rise Time		2	5	7	nS
$t_{d(off)}$	Turn-Off Delay Time		30	67	100	nS
t_f	Fall Time		2	4.5	12	nS
Q_g	Total Gate Charge	V_{GS}=10V, I_D=20A, V_{DS}=480V	65	87	114	nC
Q_{gs}	Gate-to-Source Charge		6	11	13	nC
Q_{gd}	Gate-to-Drain Charge		23	33	36	nC
$V_{(plateau)}$	Gate Plateau voltage		2	5.5	7	V
t_{rr}	Source-to-Drain Reverse Recovery Time	I_S=I_F, di/dt=100A/uS, Vrr=480V	100	200	250	nS
Qrr	Reverse recovery charge		7	11	14	μC
Irm	Peak reverse recovery current		30	70	80	A
V_{SD}	Diode Forward Voltage	I_S=IF, V_{GS}=0V	0.5	1.0	1.2	V

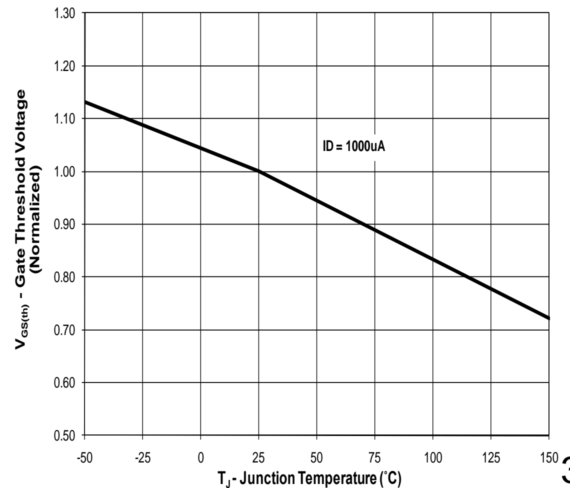

Output Characteristics
I_D - Drain Current (A)
V_{DS} - Drain-to-Source Voltage (V)
V_{GS} = 10V
9V
8 V
7 V
6 V

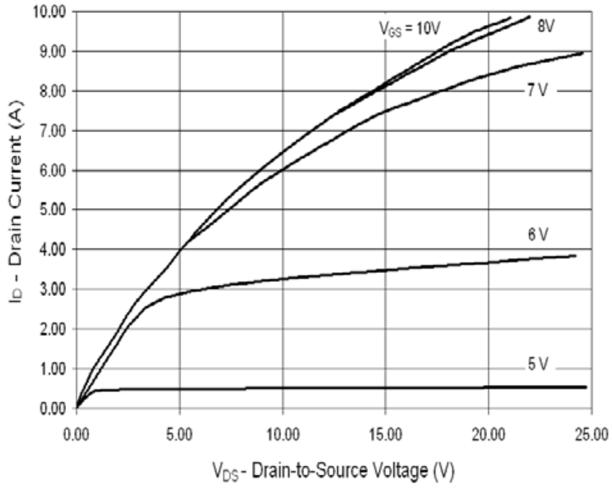

Transfer Characteristics
ID - Drain Current (A)
VGS - Gate-to-Source (V)
TJ = 125˚C
25˚C
-55˚C

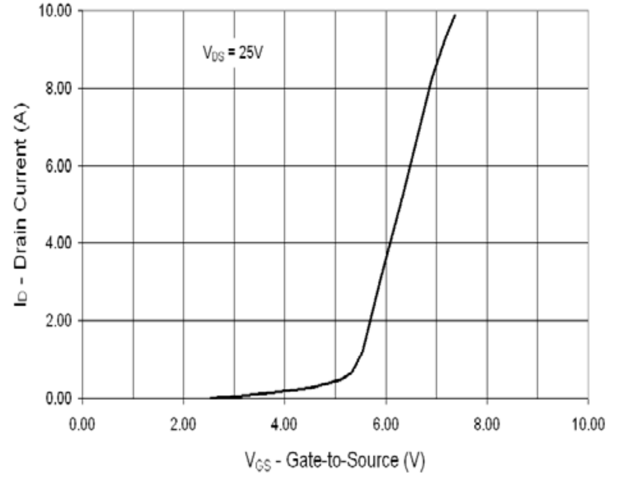

On State Resistance vs. Drain Current
rDS(on) - On State Resistance (mΩ)
I_D - Drain Current (A)
V_{GS} = 10V

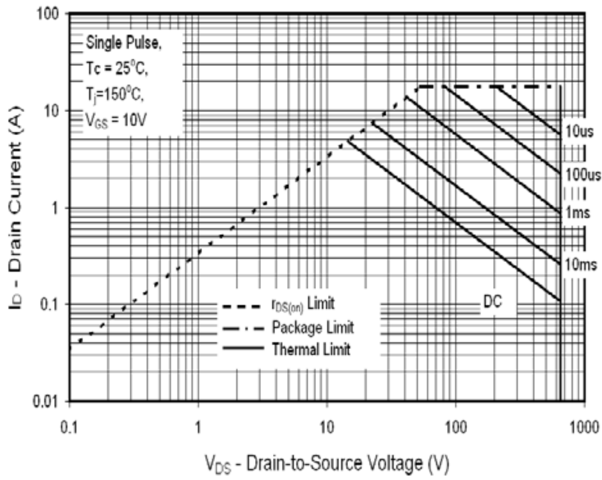

On-State Resistance vs. Junction Temperature
$R_{DS(on)}$ - On-State Resistance (Normalized)
T_J - Junction Temperature (˚C)
V_{GS} = 10V
I_D = 20 A

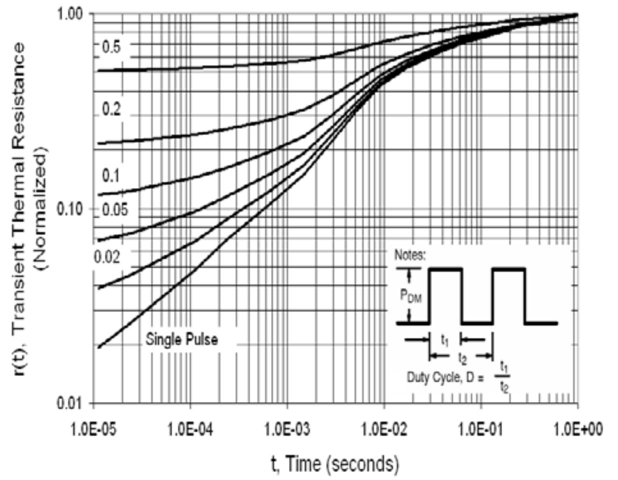

On-Resistance vs. Gate-to-Source Voltage
$R_{DS(on)}$ - On State Resistance (Ω)
V_{GS} - Gate-to-Source Voltage (V)
I_D = 10 A

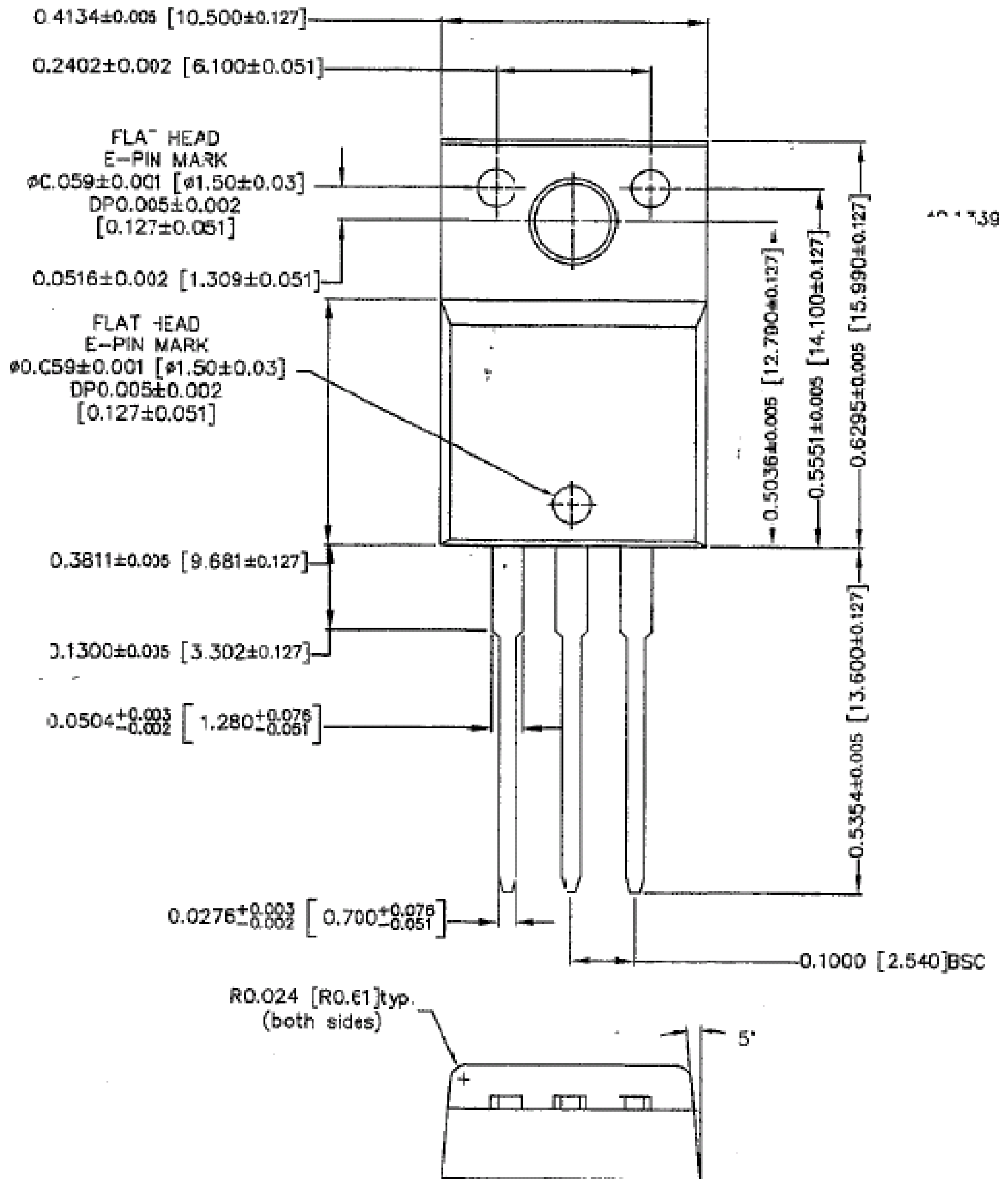

Gate Threshold Voltage vs. Junction Temperature
$V_{GS(th)}$ - Gate Threshold Voltage (Normalized)
T_J - Junction Temperature (˚C)
ID = 1000uA

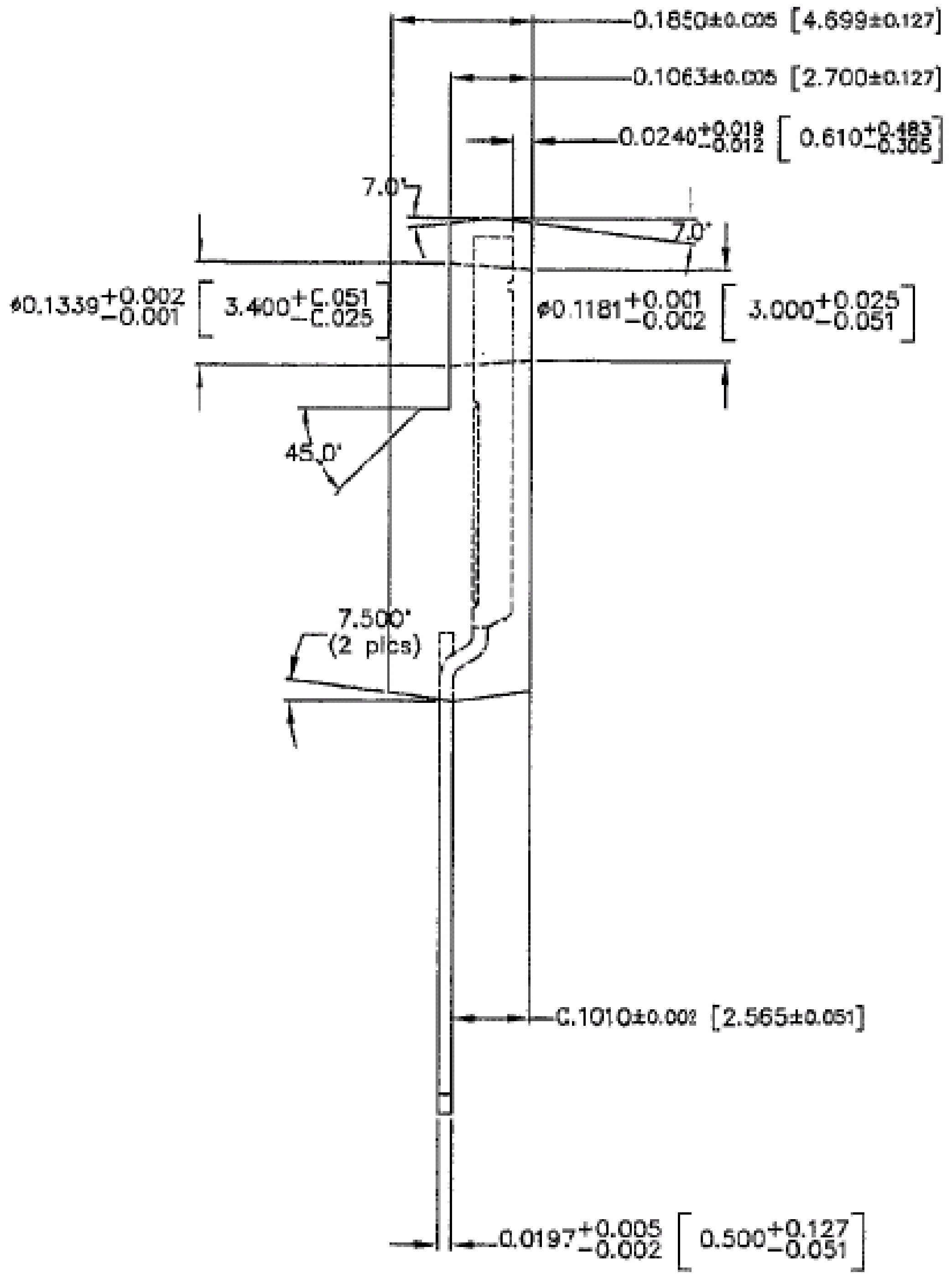

Output Characteristics
V_{GS} = 10V
8V
7 V
6 V
5 V
I_D - Drain Current (A)
V_{DS} - Drain-to-Source Voltage (V)
10.00
9.00
8.00
7.00
6.00
5.00
4.00
3.00
2.00
1.00
0.00
5.00
10.00
15.00
20.00
25.00

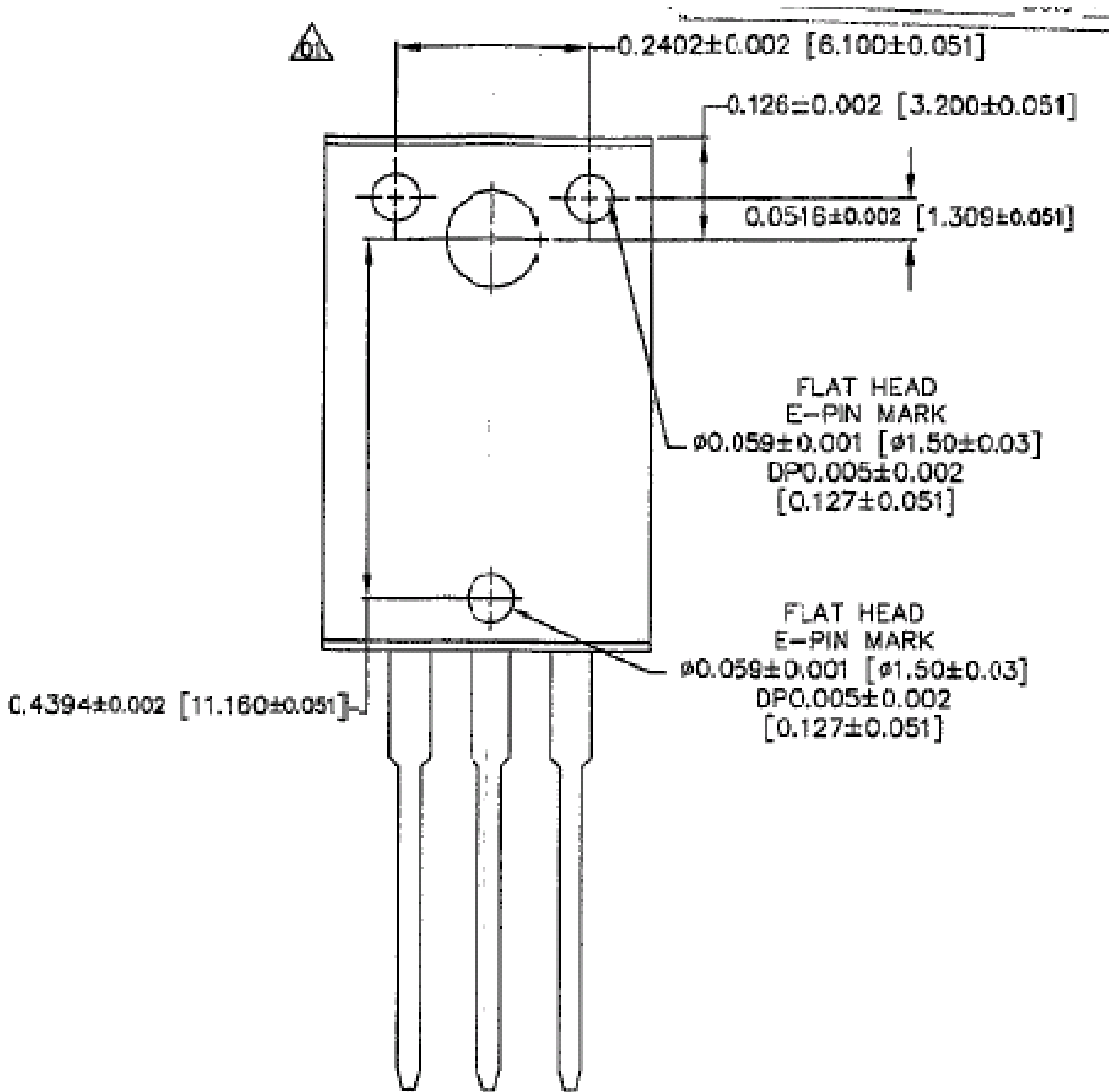

Transfer Characteristics
V_{DS} = 25V
I_D - Drain Current (A)
V_{GS} - Gate-to-Source (V)
10.00
8.00
6.00
4.00
2.00
0.00


Maximum Rated Forward Biased Safe Operating Area
Single Pulse,
Tc = 25°C,
Tj=150°C,
VGS = 10V
10us
100us
1ms
10ms
DC
rDS(on) Limit
Package Limit
Thermal Limit
ID - Drain Current (A)
VDS - Drain-to-Source Voltage (V)
100
10
1
0.1
0.01
0.1
1
10
100
1000


Transient Thermal Response, Junction-to-Case
r(t), Transient Thermal Resistance (Normalized)
t, Time (seconds)
1.00
0.10
0.01
0.5
0.2
0.1
0.05
0.02
Single Pulse
Notes:
PDM
t1
t2
Duty Cycle, D = t1/t2
1.0E-05
1.0E-04
1.0E-03
1.0E-02
1.0E-01
1.0E+00


0.4134±0.005 [10.500±0.127]
0.2402±0.002 [6.100±0.051]
FLAT HEAD
E-PIN MARK
ø0.059±0.001 [ø1.50±0.03]
DP0.005±0.002
[0.127±0.051]
0.0516±0.002 [1.309±0.051]
FLAT HEAD
E-PIN MARK
ø0.059±0.001 [ø1.50±0.03]
DP0.005±0.002
[0.127±0.051]
0.3811±0.005 [9.681±0.127]
0.1300±0.005 [3.302±0.127]
0.0504+0.003/-0.002 [1.280+0.076/-0.051]
0.0276+0.003/-0.002 [0.700+0.076/-0.051]
0.1000 [2.540]BSC
0.5036±0.005 [12.790±0.127]
0.5551±0.005 [14.100±0.127]
0.6295±0.005 [15.990±0.127]
0.5354±0.005 [13.600±0.127]
R0.024 [R0.61]typ.
(both sides)
5°


0.1850±0.005 [4.699±0.127]
0.1063±0.005 [2.700±0.127]
0.0240+0.019 −0.012 [0.610+0.483 −0.305]
7.0°
7.0°
ϕ0.1339+0.002 −0.001 [3.400+0.051 −0.025]
ϕ0.1181+0.001 −0.002 [3.000+0.025 −0.051]
45.0°
7.500° (2 plcs)
0.1010±0.002 [2.565±0.051]
0.0197+0.005 −0.002 [0.500+0.127 −0.051]


0.2402±0.002 [6.100±0.051]
0.126±0.002 [3.200±0.051]
0.0516±0.002 [1.309±0.051]
FLAT HEAD
E-PIN MARK
ø0.059±0.001 [ø1.50±0.03]
DP0.005±0.002
[0.127±0.051]
FLAT HEAD
E-PIN MARK
ø0.059±0.001 [ø1.50±0.03]
DP0.005±0.002
[0.127±0.051]
0.4394±0.002 [11.160±0.051]

ICEMOS SUPERJUNCTION PATENT PORTFOLIO

ICEMOS GRANTED PATENTS

US7,429,772
US7,439,178
US7,446,018
US7,579,607
US7,723,172
US7,795,045
US7,846,821
US7,944,018
US8,012,806
US8,030,133

3D SEMI PATENTS LICENSED TO ICEMOS

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US7,023,069B2
US7,364,994
US7,227,197B2
US7,304,944B2
US7,052,982B2
US7,339,252
US7,410,891
US7,439,583
US7,227,197B2
US6,635,906
US6,936,867
US7,015,104
US9,109,110
US7,271,067
US7,354,818
US7,052,982,
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.