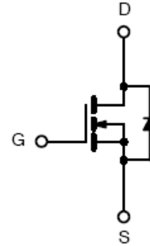
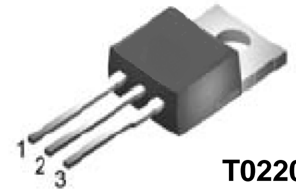
ICE20N65 N-Channel Enhancement Mode MOSFET

Product Summary			
I_D	T_A=25°C	20A	Max
$V_{(BR)DSS}$	I_D=250uA	650V	Min
$r_{DS(on)}$	V_{GS}=10V	0.17 Ω	Typ

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High dV/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems





T0220

Standard Metal Heatsink

1=Gate, 2=Drain, 3=Source.

ICEMOS HAS THE LEADERSHIP PATENT PORTFOLIO FOR SUPERJUNCTION MOSFETS (see page 9). ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA,CHINA,KOREA,JAPAN,TAIWAN,EUROPE.

Maximum Ratings and Thermal Characteristics [b] (T_A=25°C unless otherwise noted)

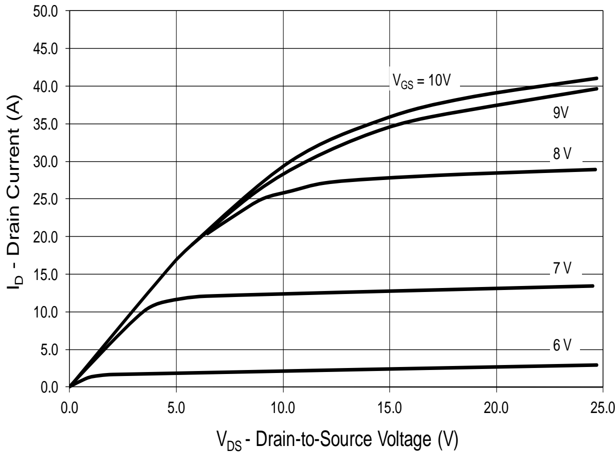
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		VDS	650	V
Gate-Source Voltage (Static)		VGS	±20	
Gate-Source Voltage AC (f > 1Hz)		VGS	±30	
Drain Current	- Continuous (Tc = 25° C)	ID	20	A
	- Pulsed (limited by Tjmax)	IDM	82	
Repetitive Avalanche Current (limited by Tjmax)		IAR	7	A
Energy in Avalanche (single pulse, ID = 3.5A)		EAS	690	mJ
Maximum Power Dissipation (Tc = 25° C)		PD	208	W
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	oC
dV/dt voltage slope (Vds=480V, ID=20A, Tj = 125 °C		dV/dt	50	V/ns
Thermal Resistance	- Junction-to-Ambient	RthJA	72	oC/W
	- Junction-to-Case	RthJC	0.6	oC/W

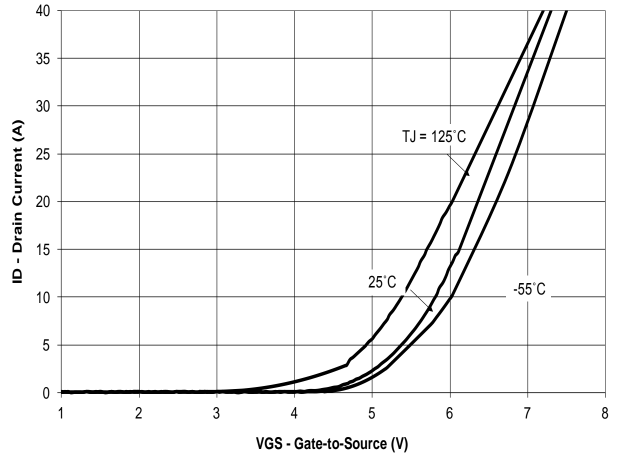
a When mounted on 1 inch square 2oz copper clad FR-4

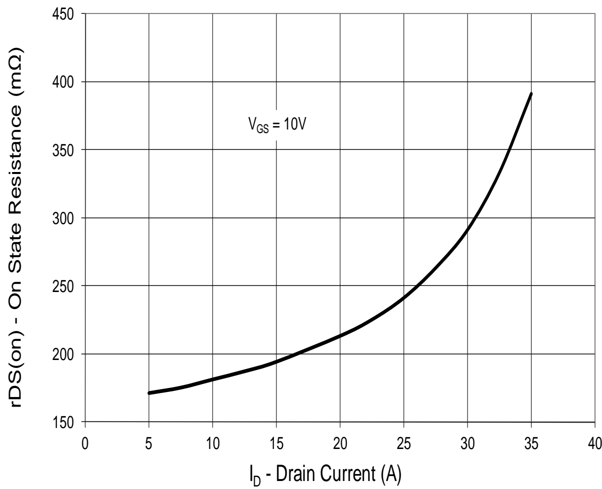
b Preliminary Data Sheet - Specifications subject to change.

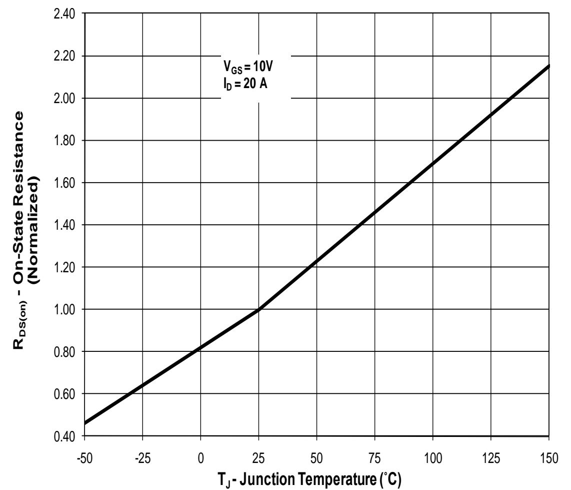
Electrical Characteristics[b] (TJ=25°C unless otherwise specified)

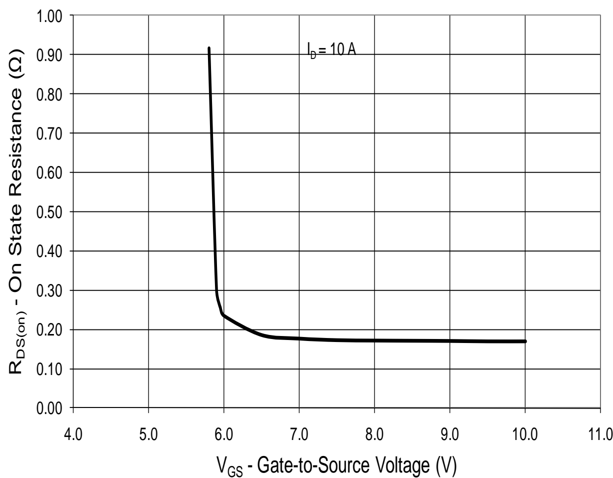
Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	650	675		V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=600V, V_{GS}=0V		0.1	1	µA
		TJ = 150°C		20	100	µA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V		10	100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2.5	3	3.5	V
$r_{DS(on)}$	Drain-to-Source On-State Resistance	V_{GS}=10V, I_D=10A	0.139	0.17	0.199	Ω
		TJ = 150°C	0.33	0.4	0.597	Ω
R_G	Gate Resistance	f = 1MHz,	0.2	0.5	0.7	Ω
g_{fs}	Transconductance	V_{DS}> 2*I_D*R_{DS} , I_D = 10A	13	20	30	S
C_{iss}	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz	900	2400	2700	pF
C_{oss}	Output Capacitance		600	780	820	pF
C_{rss}	Reverse Transfer Capacitance		20	50	70	pF
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=10V, I_D=20A, V_{DS}=380V R_G = 4Ω (External)	5	10	12	nS
t_r	Rise Time		2	5	7	nS
$t_{d(off)}$	Turn-Off Delay Time		30	67	100	nS
t_f	Fall Time		2	4.5	12	nS
Q_g	Total Gate Charge	V_{GS}=10V, I_D=20A, V_{DS}=480V	65	87	114	nC
Q_{gs}	Gate-to-Source Charge		6	11	13	nC
Q_{gd}	Gate-to-Drain Charge		23	33	36	nC
$V_{(plateau)}$	Gate Plateau voltage		2	5.5	7	V
t_{rr}	Source-to-Drain Reverse Recovery Time	I_S=I_F, di/dt=100A/uS, Vrr=480V	100	200	250	nS
Qrr	Reverse recovery charge		7	11	14	µC
Irm	Peak reverse recovery current		30	70	80	A
V_{SD}	Diode Forward Voltage	I_S=IF, V_{GS}=0V	0.5	1.0	1.2	V

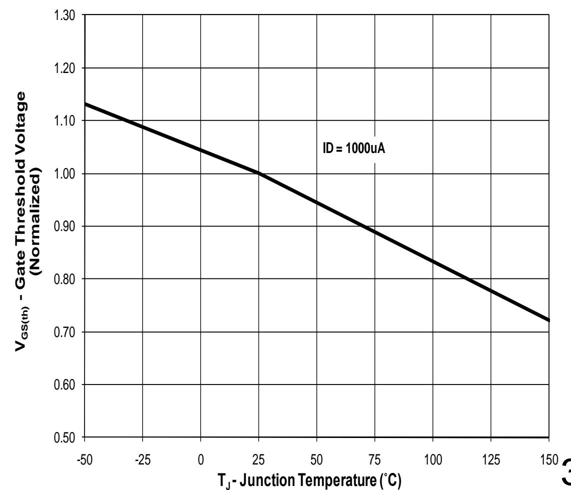

Output Characteristics
V_{GS} = 10V
9V
8 V
7 V
6 V
I_D - Drain Current (A)
V_{DS} - Drain-to-Source Voltage (V)
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
45.0
50.0

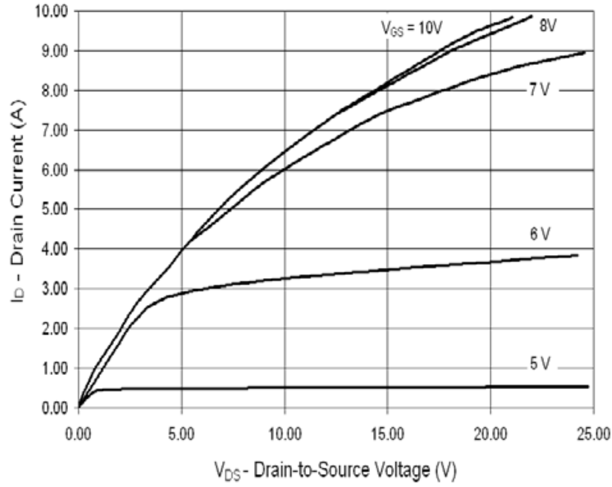

Transfer Characteristics
TJ = 125˚C
25˚C
-55˚C
ID - Drain Current (A)
VGS - Gate-to-Source (V)

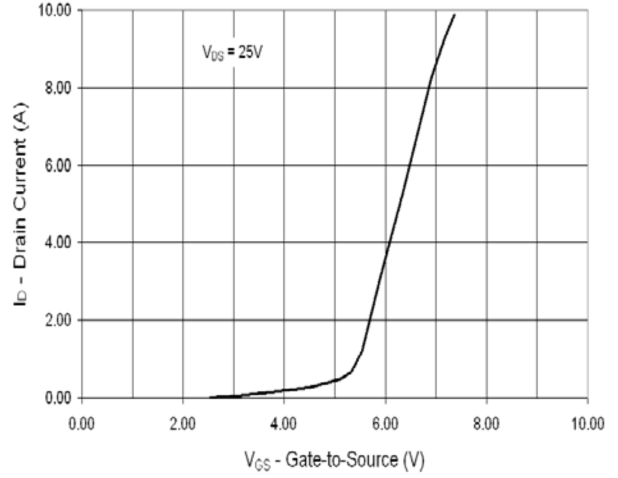

On State Resistance vs. Drain Current
V_{GS} = 10V
rDS(on) - On State Resistance (mΩ)
I_D - Drain Current (A)

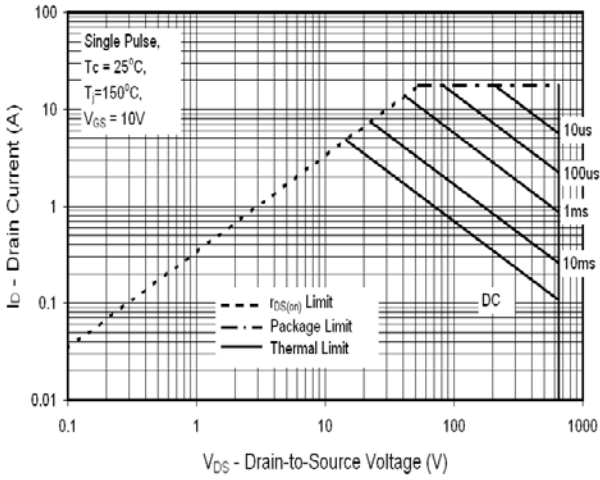

On-State Resistance vs. Junction Temperature
V_{GS} = 10V
I_D = 20 A
$R_{DS(on)}$ - On-State Resistance (Normalized)
T_J - Junction Temperature (˚C)

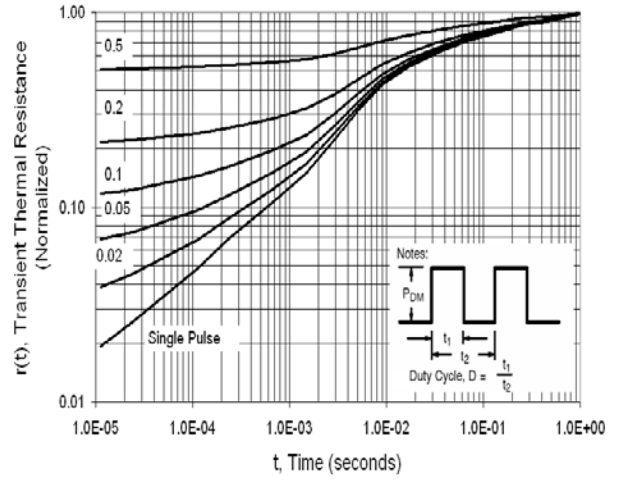

On-Resistance vs. Gate-to-Source Voltage
I_D = 10 A
$R_{DS(on)}$ - On State Resistance (Ω)
V_{GS} - Gate-to-Source Voltage (V)

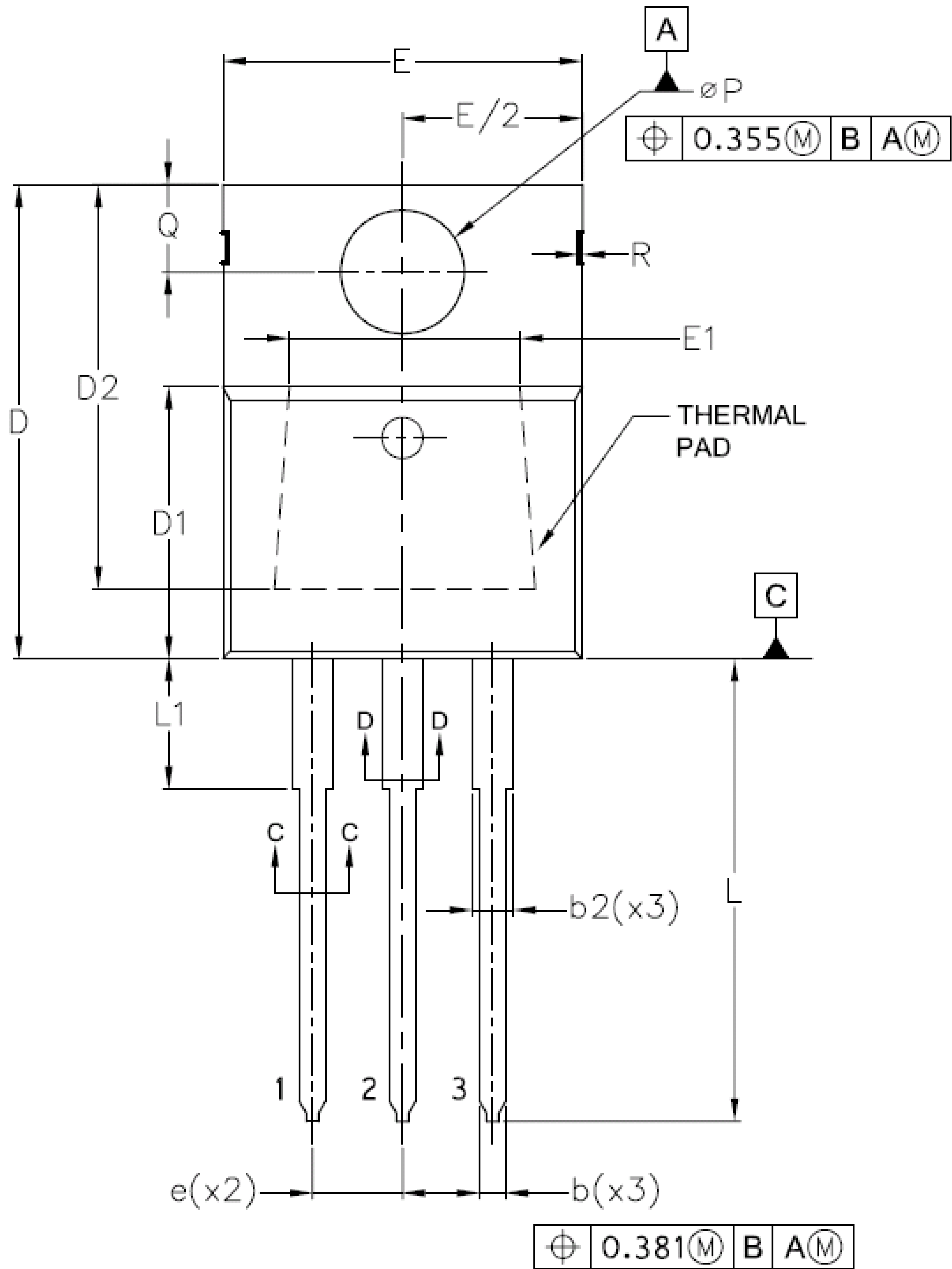

Gate Threshold Voltage vs. Junction Temperature
ID = 1000uA
$V_{GS(th)}$ - Gate Threshold Voltage (Normalized)
T_J - Junction Temperature (˚C)

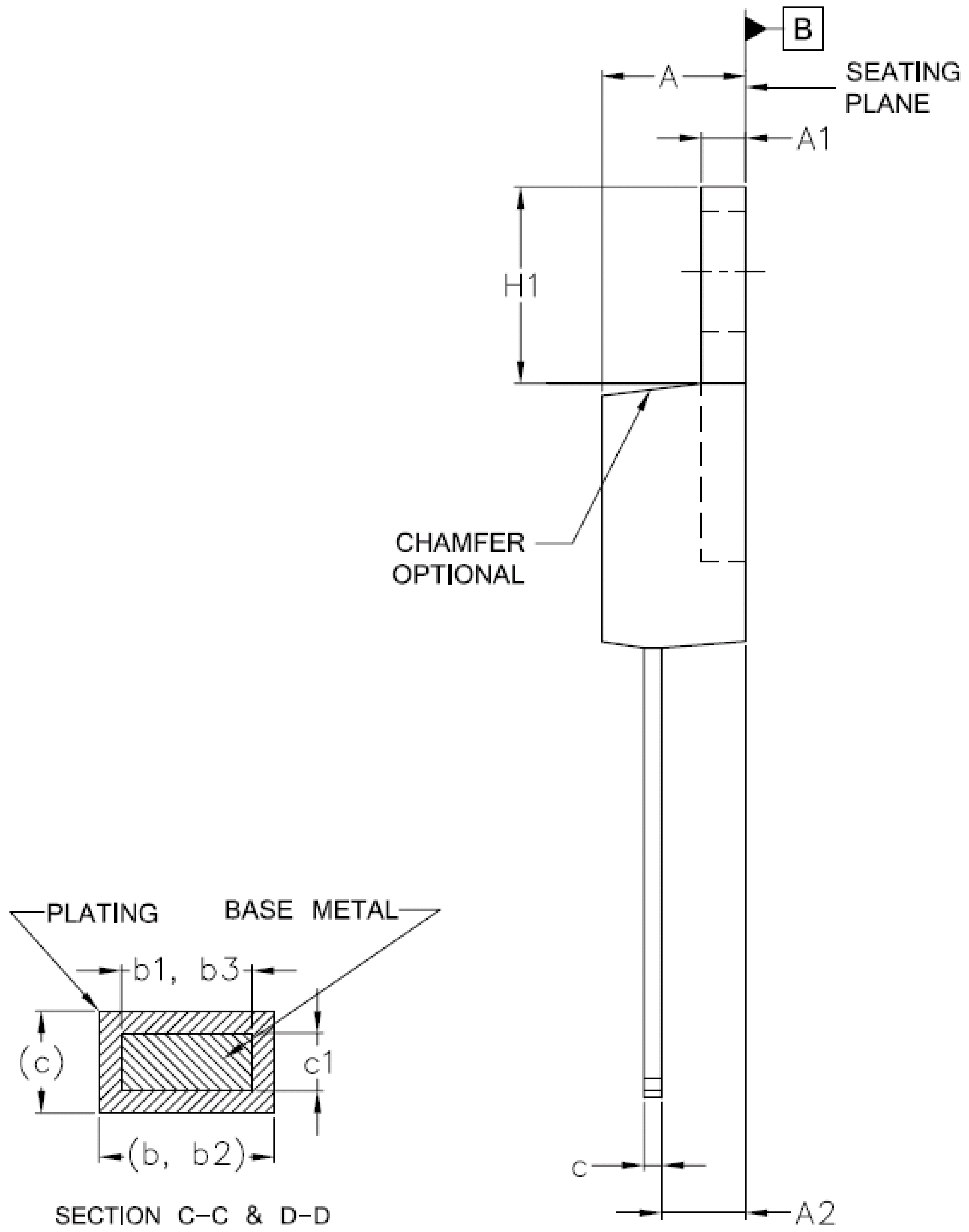

Output Characteristics
V_{GS} = 10V
8V
7 V
6 V
5 V
I_D - Drain Current (A)
V_{DS} - Drain-to-Source Voltage (V)
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.00
0.00
5.00
10.00
15.00
20.00
25.00


Transfer Characteristics
V_{DS} = 25V
I_D - Drain Current (A)
V_{GS} - Gate-to-Source (V)
0.00
2.00
4.00
6.00
8.00
10.00
0.00
2.00
4.00
6.00
8.00
10.00


Maximum Rated Forward Biased Safe Operating Area
Single Pulse,
Tc = 25°C,
Tj=150°C,
VGS = 10V
10us
100us
1ms
10ms
DC
rDS(on) Limit
Package Limit
Thermal Limit
ID - Drain Current (A)
VDS - Drain-to-Source Voltage (V)


Transient Thermal Response, Junction-to-Case
0.5
0.2
0.1
0.05
0.02
Single Pulse
Notes:
PDM
t1
t2
Duty Cycle, D = t1/t2
r(t), Transient Thermal Resistance (Normalized)
t, Time (seconds)


A
E
E/2
øP
0.355Ⓜ B AⓂ
Q
R
E1
D2
D
THERMAL
PAD
D1
C
L1
D D
C C
b2(x3)
L
1 2 3
e(x2)
b(x3)
0.381Ⓜ B AⓂ


B
A
SEATING
PLANE
A1
H1
CHAMFER
OPTIONAL
PLATING
BASE METAL
b1, b3
(c)
c1
(b, b2)
SECTION C-C & D-D
c
A2

SYMBOLS	DIMENSIONS			
	mm		Inch	
	MIN.	MAX.	MIN.	MAX.
A	3.556	4.826	0.140	0.190
A1	0.508	1.397	0.020	0.055
A2	2.032	2.921	0.080	0.115
b	0.381	1.016	0.015	0.040
b1	0.381	0.965	0.015	0.038
c	0.356	0.610	0.014	0.024
c1	0.356	0.559	0.014	0.022
D	14.224	16.510	0.560	0.650
D1	8.382	9.017	0.330	0.355
D2	12.192	12.878	0.480	0.507
E	9.652	10.668	0.380	0.420
E1	6.858	8.890	0.270	0.350
e	2.540 BSC		0.100 BSC	
H1	5.842	6.858	0.230	0.270
L	12.700	14.732	0.500	0.580
⌀P	3.810	3.860	0.150	0.151
Q	2.540	3.048	0.100	0.120
b2	1.143	1.778	0.045	0.070
R	1.270 BSC		0.050 BSC	
L1	–	6.350	–	0.250
b3	1.143	1.727	0.045	0.068
f1	3.200 REF.		0.126 REF.	
f2	4.220 REF.		0.166 REF.	
j	1.750 REF.		0.069 REF.	
r	0.510 REF.		0.020 REF.	
N	TO-220-3L			

ICEMOS SUPERJUNCTION PATENT PORTFOLIO

ICEMOS GRANTED PATENTS

US7,429,772
US7,439,178
US7,446,018
US7,579,607
US7,723,172
US7,795,045
US7,846,821
US7,944,018
US8,012,806
US8,030,133

3D SEMI PATENTS LICENSED TO ICEMOS

US7,041,560B2
US7,023,069B2
US7,364,994
US7,227,197B2
US7,304,944B2
US7,052,982B2
US7,339,252
US7,410,891
US7,439,583
US7,227,197B2
US6,635,906
US6,936,867
US7,015,104
US9,109,110
US7,271,067
US7,354,818
US7,052,982,
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.