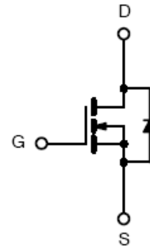
Icemos
Cooler than cool

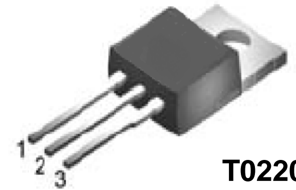
ICE20N170 N-Channel Enhancement Mode MOSFET

Product Summary			
I_D	T_A=25°C	20A	Max
$V_{(BR)DSS}$	I_D=250uA	600V	Min
$r_{DS(on)}$	V_{GS}=10V	170mΩ	Typical

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High dV/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems





T0220

Standard Metal Heatsink

1=Gate, 2=Drain, 3=Source.

ICEMOS HAS THE LEADERSHIP PATENT PORTFOLIO FOR SUPERJUNCTION MOSFETS (see page 9). ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA,CHINA,KOREA,JAPAN,TAIWAN,EUROPE.

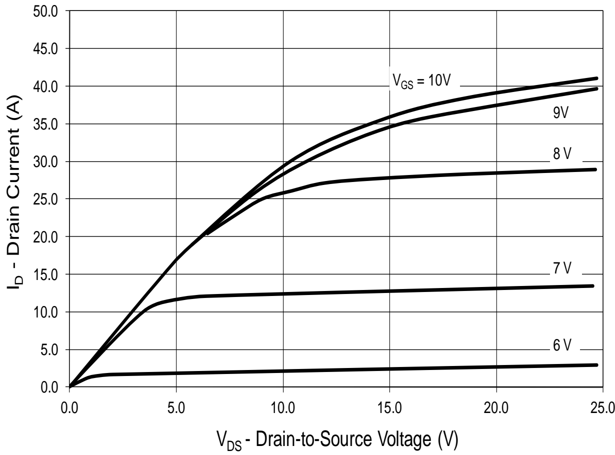
Maximum Ratings and Thermal Characteristics [b] (T_A=25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage (Static)		V_{GS}	±20	
Gate-Source Voltage AC (f > 1Hz)		V_{GS}	±30	
Drain Current	- Continuous (Tc = 25° C)	I_D	20	A
	- Pulsed (limited by Tjmax)	I_{DM}	62	
Repetitive Avalanche Current (limited by Tjmax)		I_{AR}	10	A
Energy in Avalanche (single pulse, ID = 10A)		EAS	520	mJ
Maximum Power Dissipation (Tc = 25° C)		P_D	208	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
dV/dt voltage slope (Vds=480V, ID=20A, Tj = 125 °C		dV/dt	50.0	V/ns
Thermal Resistance[a]	- Junction-to-Ambient	R_{thJA}	62	°C/W
	- Junction-to-Case	R_{thJC}	1.60	

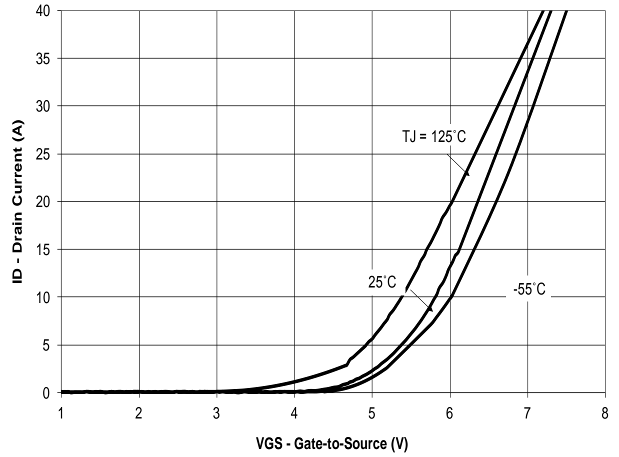
Electrical Characteristics[b] (TJ=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	600	640		V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=600V, V_{GS}=0V		0.1	1	μA
		TJ = 150°C			100	μA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2.1	3	3.9	V
$r_{DS(on)}$	Drain-to-Source On-State Resistance	V_{GS}=10V, I_D=10A	150	170	190	mΩ
		TJ = 150°C	300	430	600	mΩ
R_G	Gate Resistance	f = 1MHz,	0.2	0.5	0.7	Ω
g_{fs}	Transconductance	V_{DS}> 2*I_D*R_{DS} , I_D = 10A	12	17.5	27	S
C_{iss}	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		1800		pF
C_{oss}	Output Capacitance			590		pF
C_{rss}	Reverse Transfer Capacitance			38		pF
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=10V, I_D=20A, V_{DS}=380V R_G = 4Ω (External)	3	6	10	nS
t_r	Rise Time		2	3.5	5	nS
$t_{d(off)}$	Turn-Off Delay Time		29	54	100	nS
t_f	Fall Time		2	7	15	nS
Q_g	Total Gate Charge	V_{GS}=10V, I_D=20A, V_{DS}=480V		65		nC
Q_{gs}	Gate-to-Source Charge			13		nC
Q_{gd}	Gate-to-Drain Charge			18		nC
$V_{(plateau)}$	Gate Plateau voltage		1.9	4.7	6.8	V
t_{rr}	Source-to-Drain Reverse Recovery Time	I_S=I_F, di/dt=100A/uS, Vrr=480V	150	300	500	nS
Qrr	Reverse recovery charge		9	10	12	μC
Irm	Peak reverse recovery current		50	60	70	A
V_{SD}	Diode Forward Voltage	I_S=IF, V_{GS}=0V	0.7	0.9	1.2	V

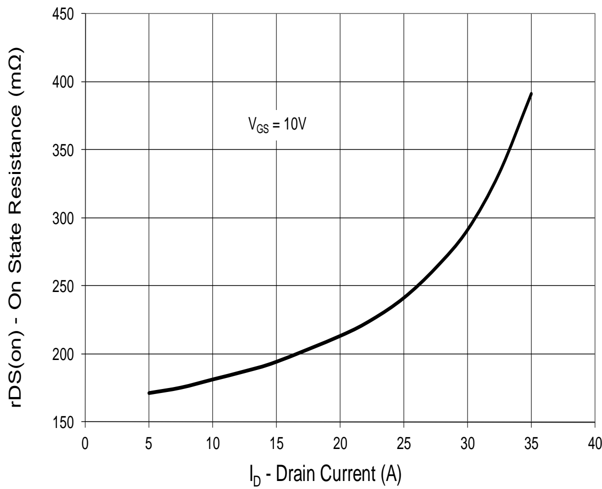
Output Characteristics



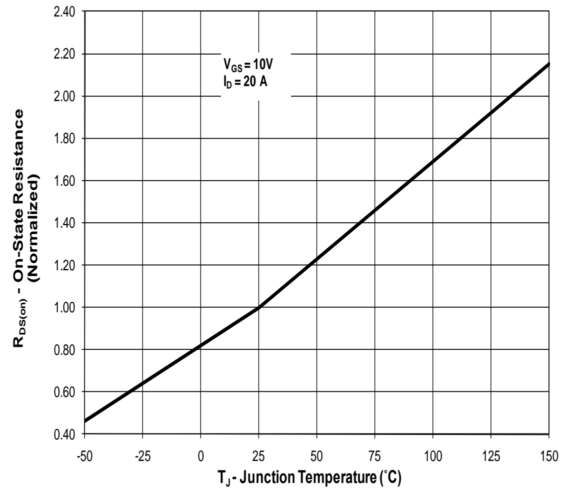
Transfer Characteristics



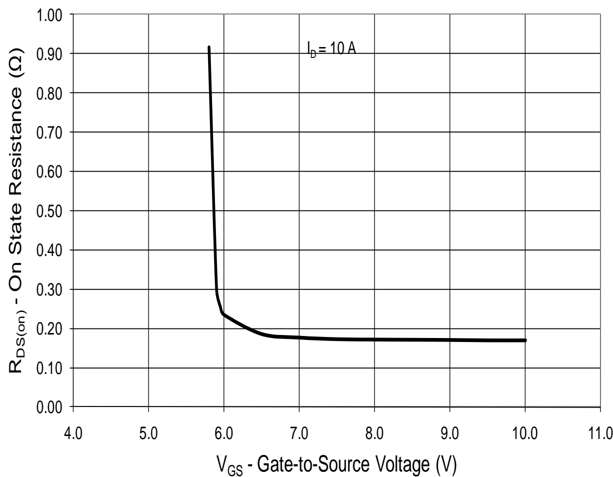
On State Resistance vs. Drain Current



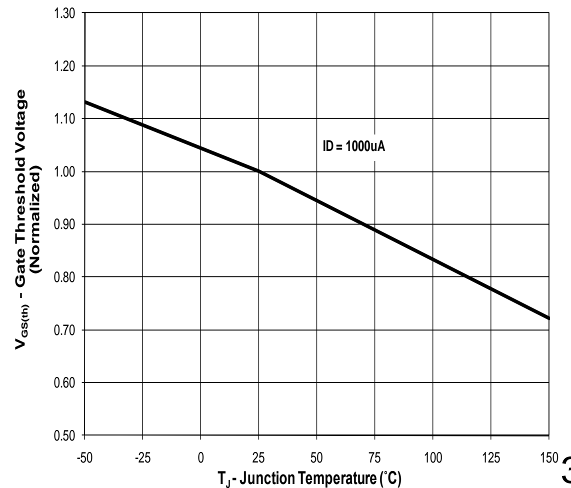
On-State Resistance vs. Junction Temperature

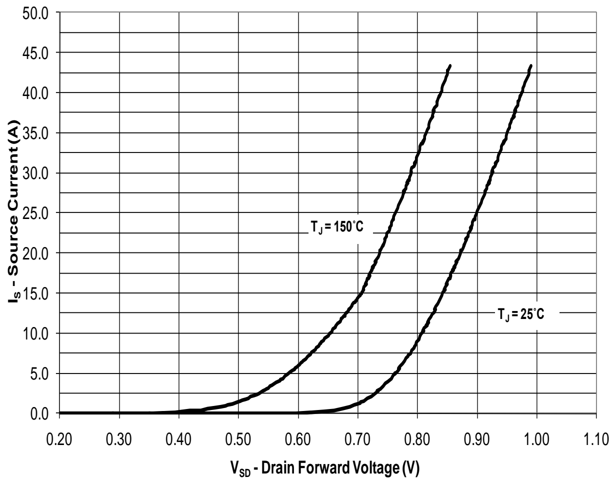


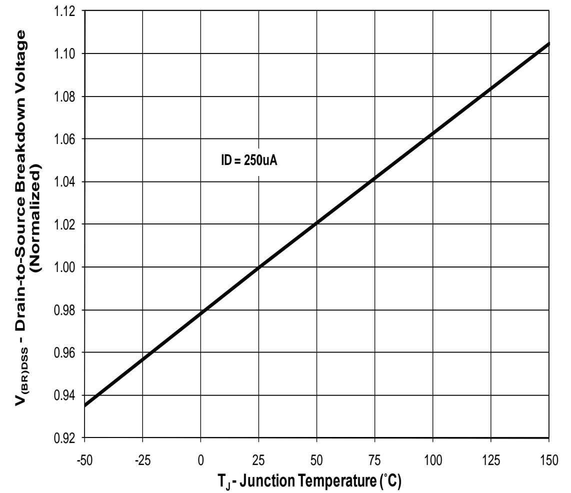
On-Resistance vs. Gate-to-Source Voltage

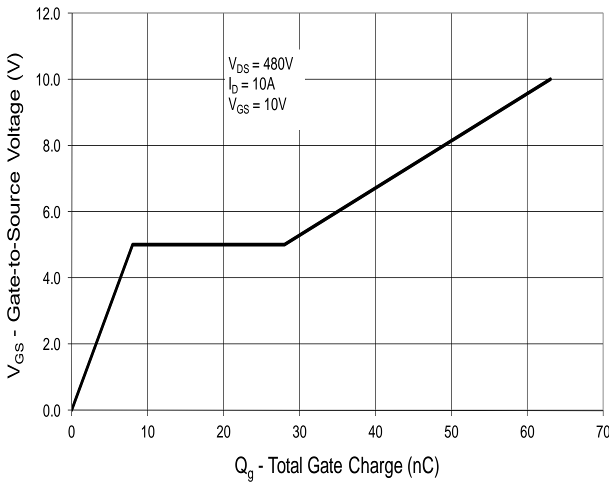


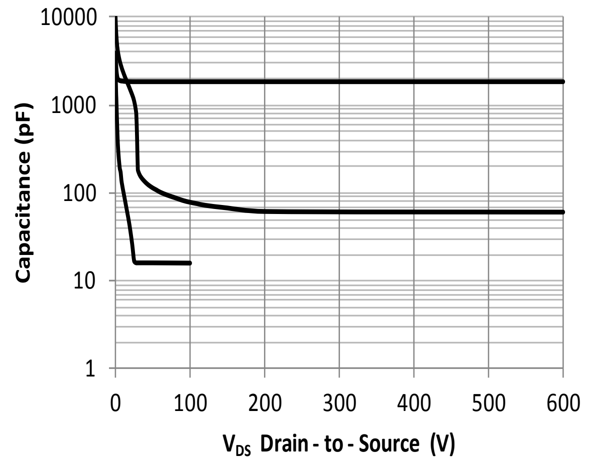
Gate Threshold Voltage vs. Junction Temperature

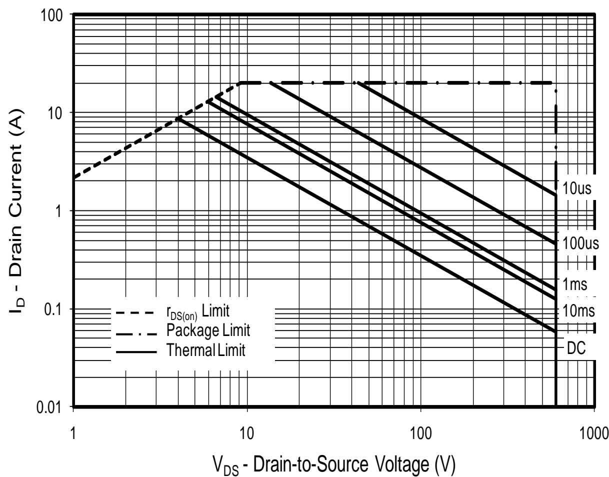


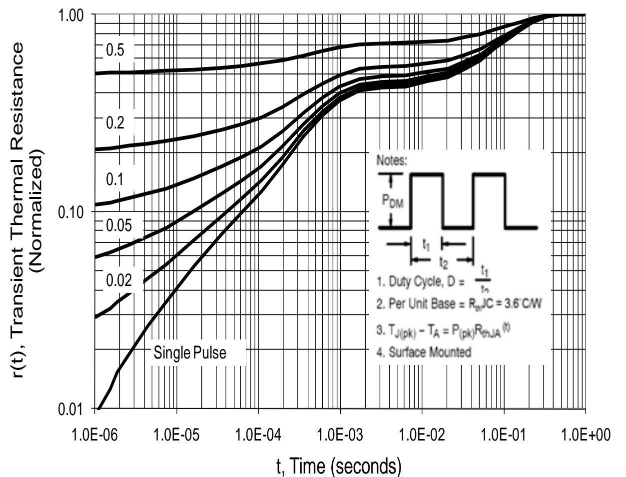

Source-Drain Forward Voltage
I_S - Source Current (A)
V_{SD} - Drain Forward Voltage (V)
T_J = 150°C
T_J = 25°C

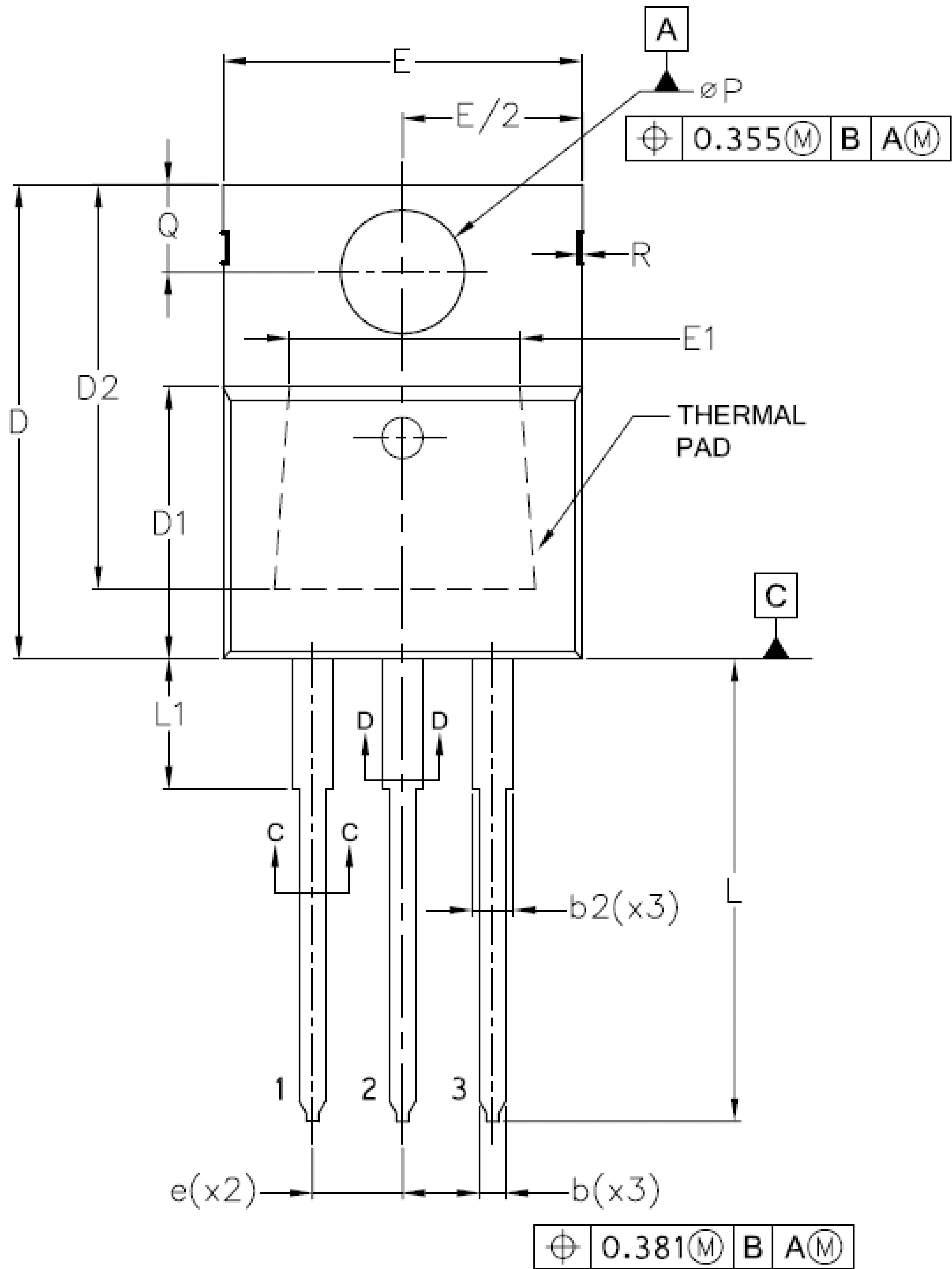

Drain-to-Source Breakdown Voltage vs. Junction Temperature
$V_{(BR)DSS}$ - Drain-to-Source Breakdown Voltage (Normalized)
ID = 250uA
T_J - Junction Temperature (°C)

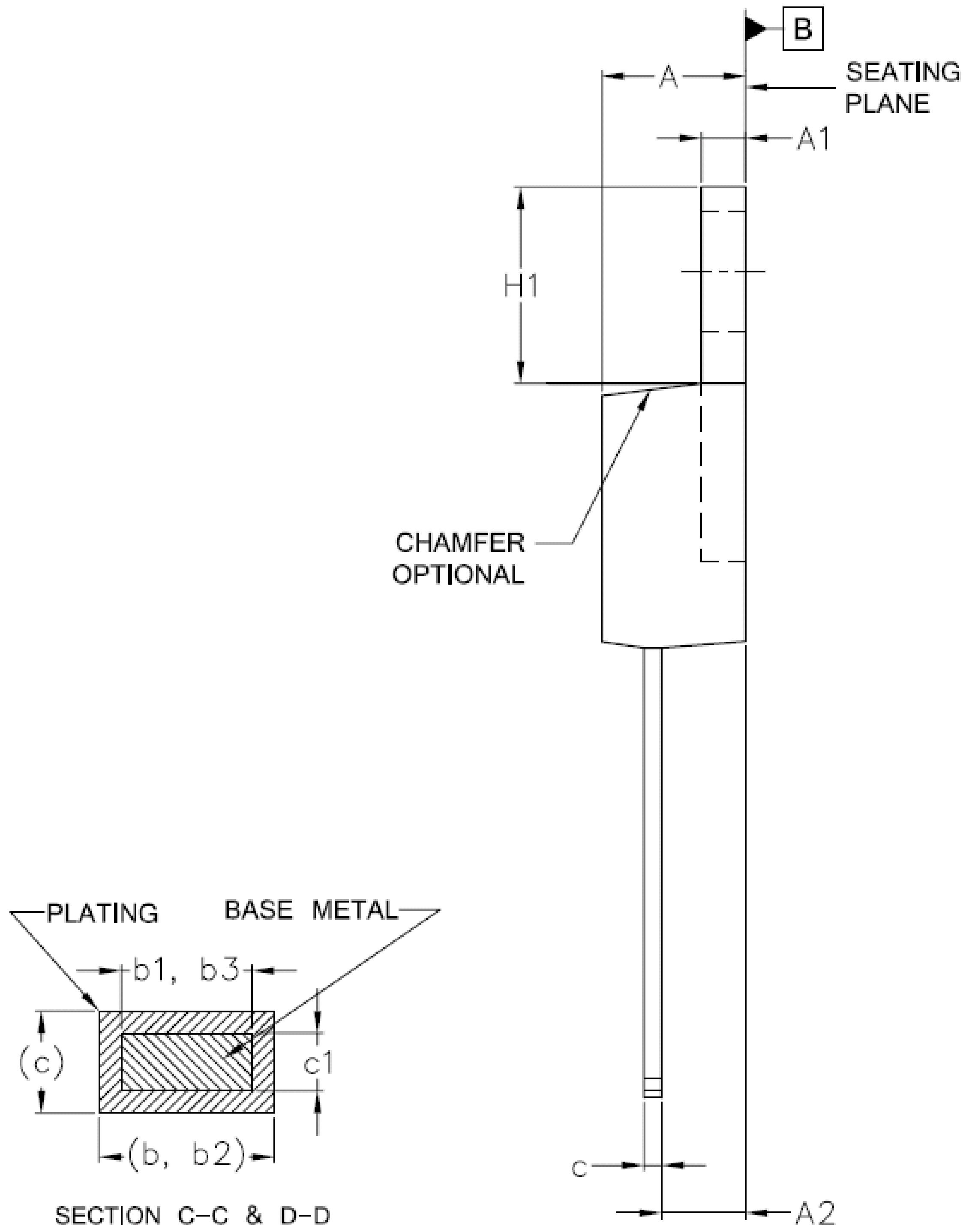

Gate Charge
V_{GS} - Gate-to-Source Voltage (V)
V_{DS} = 480V
I_D = 10A
V_{GS} = 10V
Q_g - Total Gate Charge (nC)


Capacitance
Capacitance (pF)
V_{DS} Drain - to - Source (V)


Maximum Rated Forward Biased Safe Operating Area
I_D - Drain Current (A)
$r_{DS(on)}$ Limit
Package Limit
Thermal Limit
10us
100us
1ms
10ms
DC
V_{DS} - Drain-to-Source Voltage (V)


Transient Thermal Response, Junction-to-Case
r(t), Transient Thermal Resistance (Normalized)
0.5
0.2
0.1
0.05
0.02
Single Pulse
Notes:
1. Duty Cycle, D = t1/t2
2. Per Unit Base = RthJC = 3.6°C/W
3. TJ(pk) - TA = P(pk)RthJA(t)
4. Surface Mounted
t, Time (seconds)


A
E
E/2
øP
0.355Ⓜ B AⓂ
Q
R
E1
D2
D
THERMAL PAD
D1
C
L1
D D
C C
b2(x3)
L
1 2 3
e(x2)
b(x3)
0.381Ⓜ B AⓂ


B
A
SEATING
PLANE
A1
H1
CHAMFER
OPTIONAL
PLATING
BASE METAL
b1, b3
(c)
c1
(b, b2)
SECTION C-C & D-D
c
A2

SYMBOLS	DIMENSIONS			
	mm		Inch	
	MIN.	MAX.	MIN.	MAX.
A	3.556	4.826	0.140	0.190
A1	0.508	1.397	0.020	0.055
A2	2.032	2.921	0.080	0.115
b	0.381	1.016	0.015	0.040
b1	0.381	0.965	0.015	0.038
c	0.356	0.610	0.014	0.024
c1	0.356	0.559	0.014	0.022
D	14.224	16.510	0.560	0.650
D1	8.382	9.017	0.330	0.355
D2	12.192	12.878	0.480	0.507
E	9.652	10.668	0.380	0.420
E1	6.858	8.890	0.270	0.350
e	2.540 BSC		0.100 BSC	
H1	5.842	6.858	0.230	0.270
L	12.700	14.732	0.500	0.580
⌀P	3.810	3.860	0.150	0.151
Q	2.540	3.048	0.100	0.120
b2	1.143	1.778	0.045	0.070
R	1.270 BSC		0.050 BSC	
L1	–	6.350	–	0.250
b3	1.143	1.727	0.045	0.068
f1	3.200 REF.		0.126 REF.	
f2	4.220 REF.		0.166 REF.	
j	1.750 REF.		0.069 REF.	
r	0.510 REF.		0.020 REF.	
N	TO-220-3L			

ICEMOS SUPERJUNCTION PATENT PORTFOLIO

ICEMOS GRANTED PATENTS

US7,429,772
US7,439,178
US7,446,018
US7,579,607
US7,723,172
US7,795,045
US7,846,821
US7,944,018
US8,012,806
US8,030,133

3D SEMI PATENTS LICENSED TO ICEMOS

US7,041,560B2
US7,023,069B2
US7,364,994
US7,227,197B2
US7,304,944B2
US7,052,982B2
US7,339,252
US7,410,891
US7,439,583
US7,227,197B2
US6,635,906
US6,936,867
US7,015,104
US9,109,110
US7,271,067
US7,354,818
US7,052,982,
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.