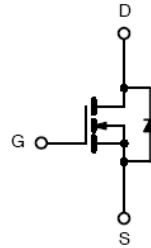


### ICE17N60FP N-Channel Enhancement Mode MOSFET

Product Summary			
$I_{D\ pulse}$	$T_A=25^\circ C$	35A	Max
$V_{(BR)DSS}$	$I_D=250\mu A$	600V	Min
$r_{DS(on)}$	$V_{GS}=10V$	193m $\Omega$	Typical

### Features

- Low  $r_{DS(on)}$
- Ultra Low Gate Charge
- High dV/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems



**ICEMOS HAS THE LEADERSHIP PATENT PORTFOLIO FOR SUPERJUNCTION MOSFETS (see page 9). ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN, EUROPE.**

**T0220  
Full-PAK  
Isolated  
(T0-220)**

### Maximum Ratings and Thermal Characteristics <sup>b</sup> ( $T_A=25^\circ C$ unless otherwise noted)

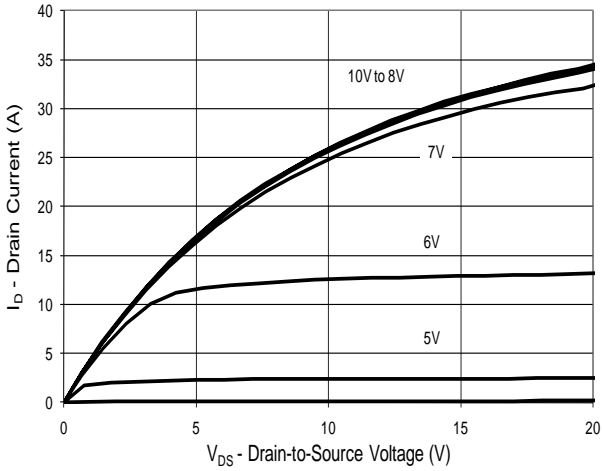
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage (Static)	$V_{GS}$	$\pm 20$	
Gate-Source Voltage AC ( $f > 1\text{Hz}$ )	$V_{GS}$	$\pm 30$	
Drain Current	- Continuous ( $T_c = 25^\circ C$ )	$I_D$	A
	- Pulsed (limited by $T_{jmax}$ )	$I_{DM}$	
Repetitive Avalanche Current (limited by $T_{jmax}$ )	$I_{AR}$	8.5	A
Energy in Avalanche (single pulse, $I_D = 8.5A$ )	EAS	460	mJ
Maximum Power Dissipation ( $T_c = 25^\circ C$ )	$P_D$	34	W
Operating Junction and Storage Temperature Range	$T_J, T_{sg}$	-55 to 150	$^\circ C$
dV/dt voltage slope ( $V_{ds}=480V, I_D=17A, T_j = 125^\circ C$ )	dV/dt	50.0	V/ns
Thermal Resistance <sup>a</sup>	- Junction-to-Ambient	$R_{thJA}$	$^\circ C/W$
	- Junction-to-Case	$R_{thJC}$	

a When mounted on 1 inch square 2oz copper clad FR-4

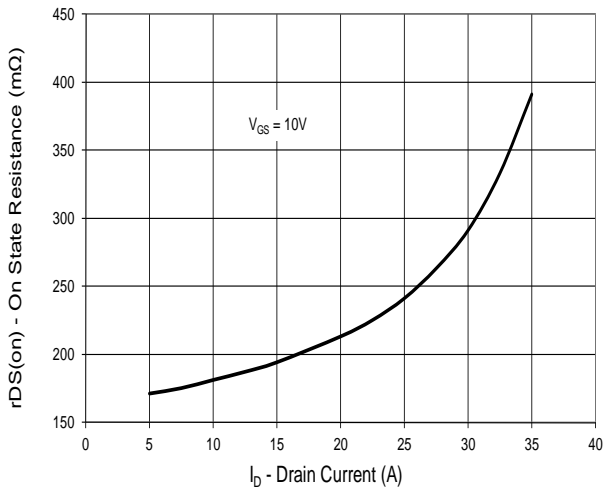
b Preliminary Data Sheet - Specifications subject to change.

**Electrical Characteristics<sup>b</sup>** (T<sub>J</sub>=25°C unless otherwise specified)

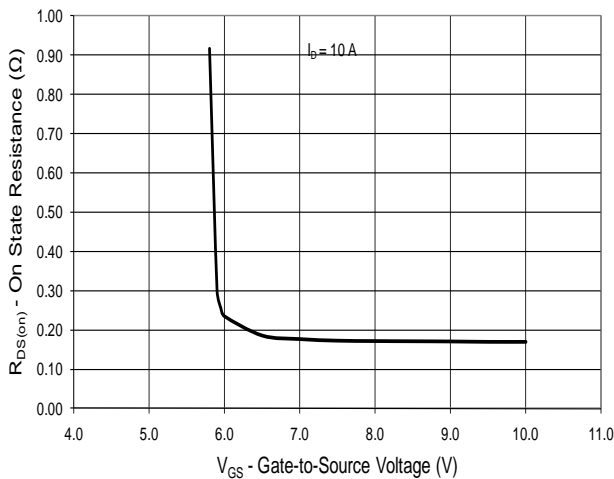
Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	600	640		V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V T <sub>J</sub> = 150°C		0.1	1	μA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	2.1	3	3.9	V
r <sub>DS(on)</sub>	Drain-to-Source On-State Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =8.5A T <sub>J</sub> = 150°C	170	193	220	mΩ
R <sub>G</sub>	Gate Resistance	f = 1MHz,	0.2	0.5	0.7	Ω
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> > 2*I <sub>D</sub> *R <sub>DS</sub> , I <sub>D</sub> = 8.5A	10	15	20	S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		1600		pF
C <sub>oss</sub>	Output Capacitance			520		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			34		pF
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, I <sub>D</sub> =17A, V <sub>DS</sub> =380V R <sub>G</sub> = 4Ω (External)	3	6	10	nS
t <sub>r</sub>	Rise Time		2	3.5	5	nS
t <sub>d(off)</sub>	Turn-Off Delay Time		29	54	100	nS
t <sub>f</sub>	Fall Time		2	7	15	nS
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =10V, I <sub>D</sub> =17A, V <sub>DS</sub> =480V		58		nC
Q <sub>gs</sub>	Gate-to-Source Charge		5	11	15	nC
Q <sub>gd</sub>	Gate-to-Drain Charge		7	15	18	nC
V <sub>(plateau)</sub>	Gate Plateau voltage		1.9	4.7	6.8	V
t <sub>rr</sub>	Source-to-Drain Reverse Recovery Time	I <sub>S</sub> =I <sub>F</sub> , di/dt=100A/uS, V <sub>rr</sub> =480V	150	300	500	nS
Q <sub>rr</sub>	Reverse recovery charge		7	9	11	μC
I <sub>rm</sub>	Peak reverse recovery current		40	50	60	A
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =I <sub>F</sub> , V <sub>GS</sub> =0V	0.7	0.9	1.2	V



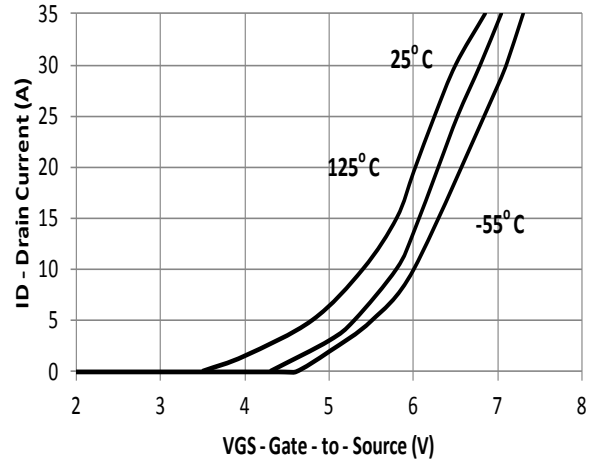
On State Resistance vs. Drain Current



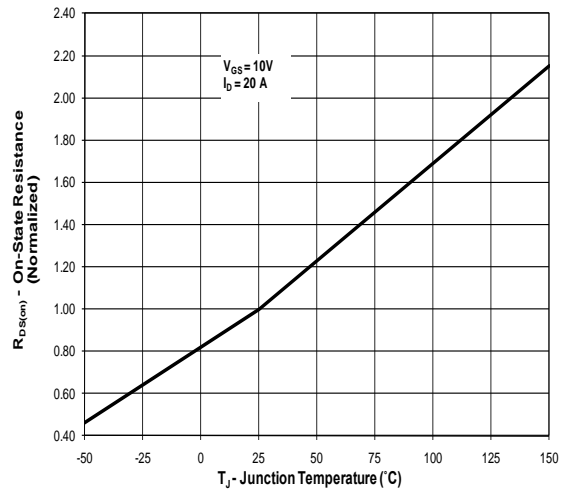
On-Resistance vs. Gate-to-Source Voltage



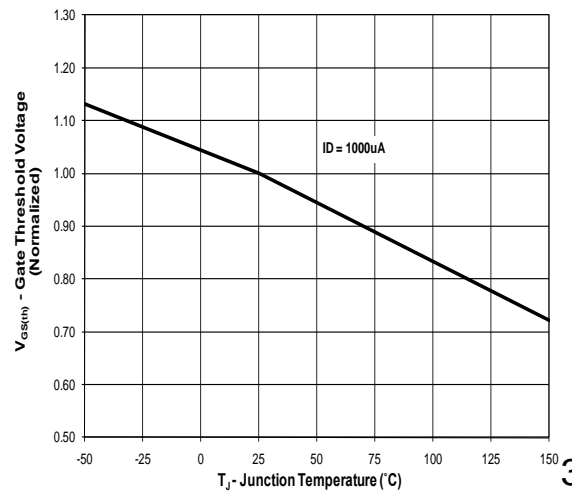
### Transfer Characteristics



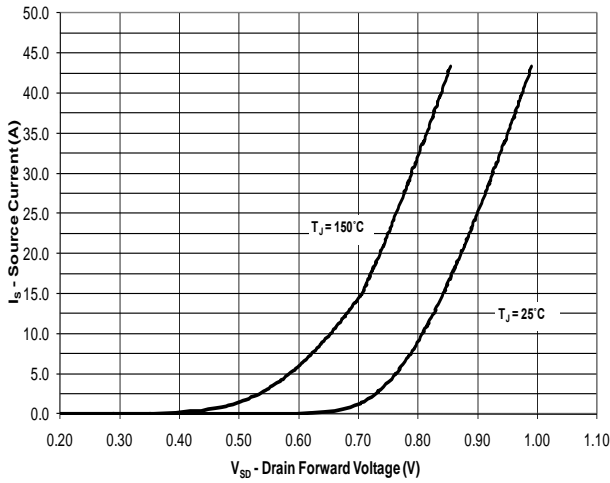
On-State Resistance vs. Junction Temperature



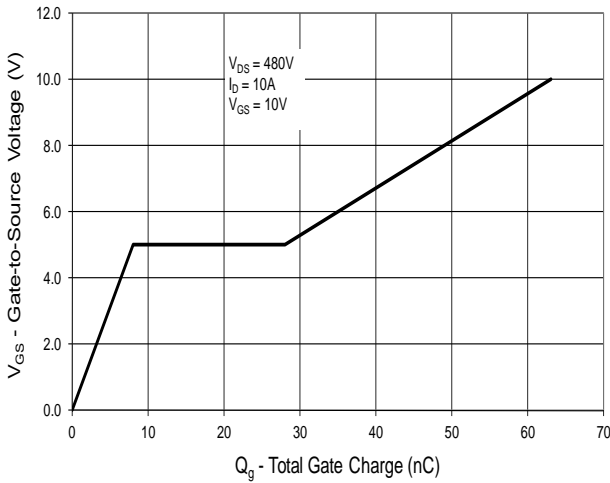
Gate Threshold Voltage vs. Junction Temperature



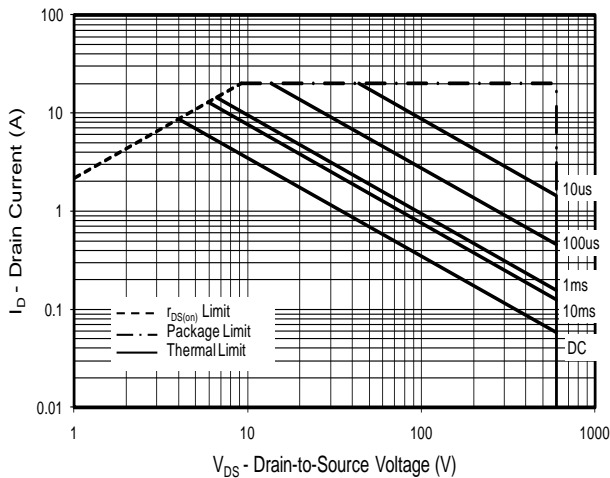
**Source-Drain Forward Voltage**



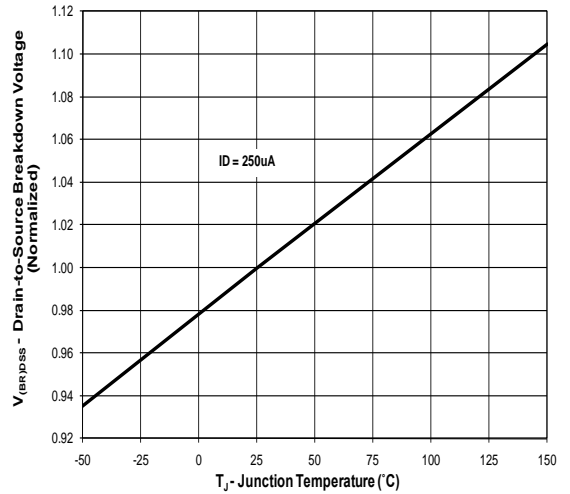
**Gate Charge**



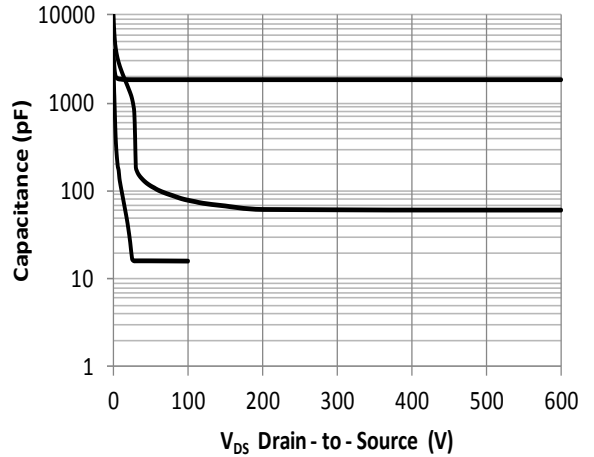
**Maximum Rated Forward Biased Safe Operating Area**



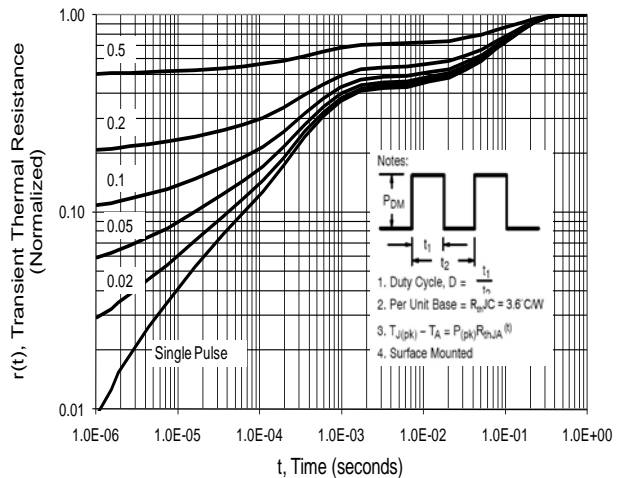
**Drain-to-Source Breakdown Voltage vs. Junction Temperature**

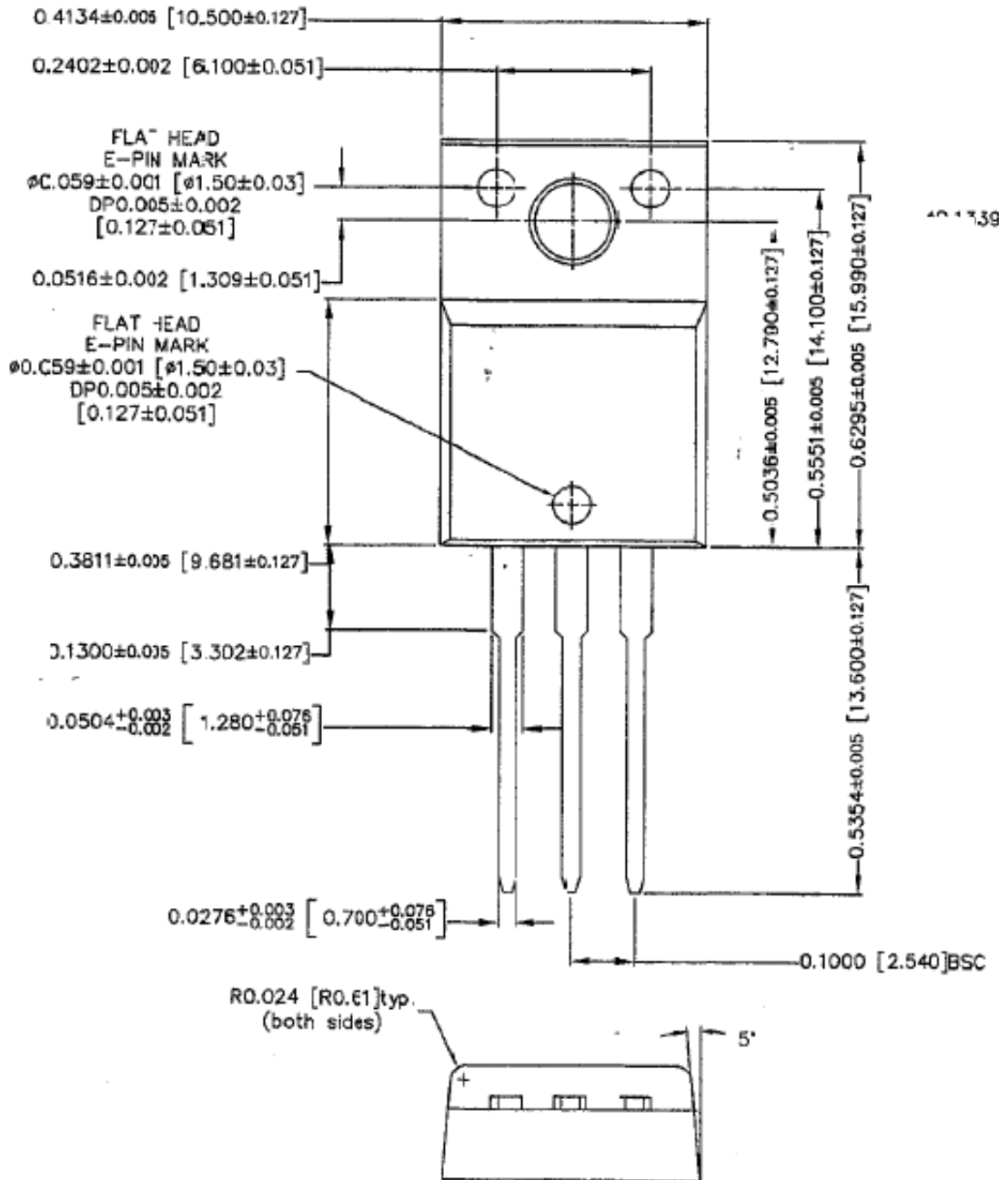


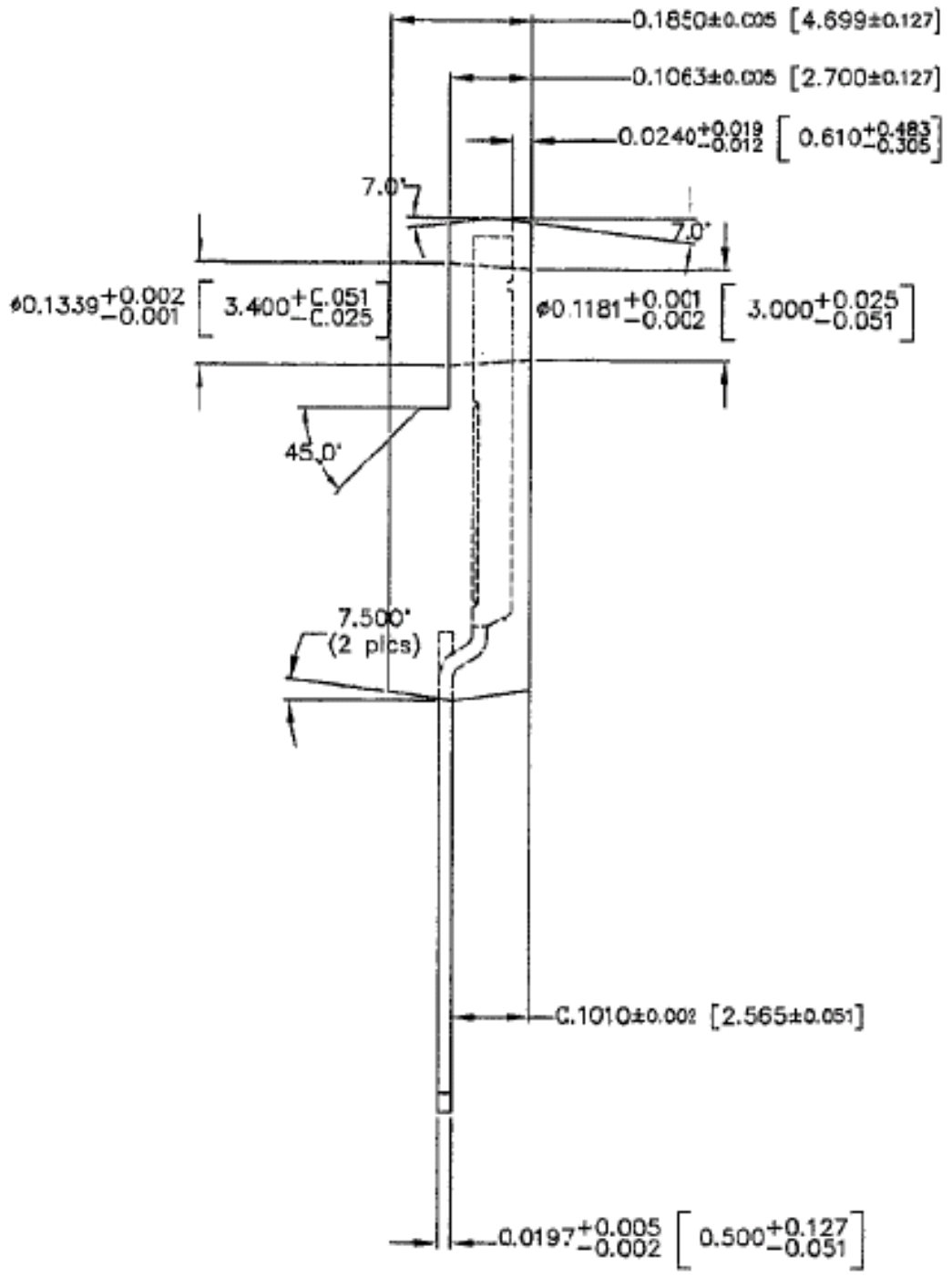
**Capacitance**

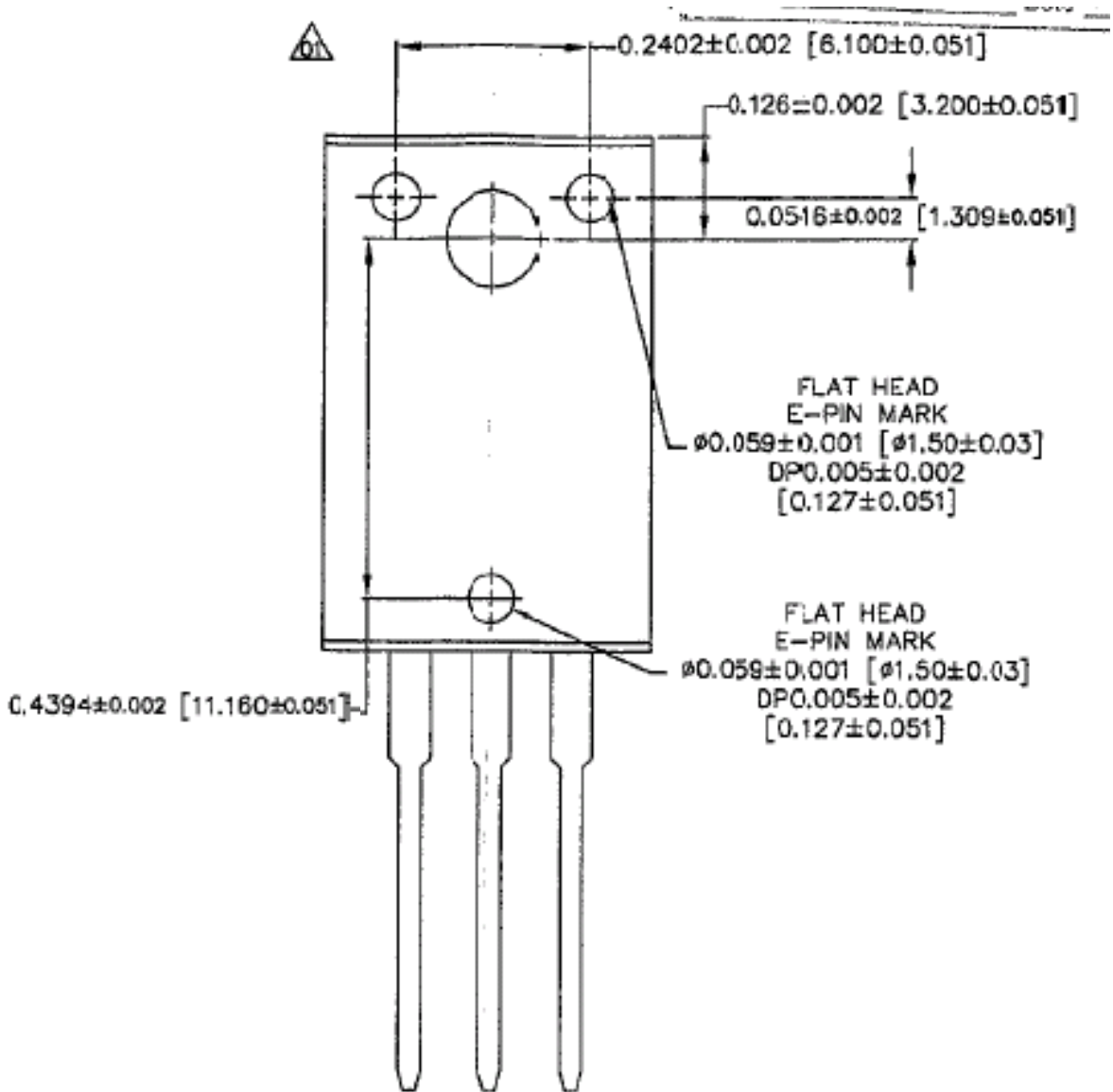


**Transient Thermal Response, Junction-to-Case**









## **ICEMOS SUPERJUNCTION PATENT PORTFOLIO**

### **ICEMOS GRANTED PATENTS**

**US7,429,772**  
**US7,439,178**  
**US7,446,018**  
**US7,579,607**  
**US7,723,172**  
**US7,795,045**  
**US7,846,821**  
**US7,944,018**  
**US8,012,806**  
**US8,030,133**

### **3D SEMI PATENTS LICENSED TO ICEMOS**

**US7,041,560B2**  
**US7,023,069B2**  
**US7,364,994**  
**US7,227,197B2**  
**US7,304,944B2**  
**US7,052,982B2**  
**US7,339,252**  
**US7,410,891**  
**US7,439,583**  
**US7,227,197B2**  
**US6,635,906**  
**US6,936,867**  
**US7,015,104**  
**US9,109,110**  
**US7,271,067**  
**US7,354,818**  
**US7,052,982,**  
**US7,199,006B2**

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.