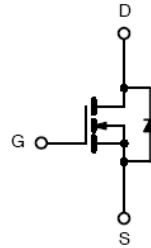


ICE11N70FP N-Channel Enhancement Mode MOSFET

Product Summary			
I_D	$T_A=25^\circ\text{C}$	11A	Max
$V_{(BR)DSS}$	$I_D=250\mu\text{A}$	700V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	0.45 Ω	Typ

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High dV/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems



ICEMOS HAS THE LEADERSHIP PATENT PORTFOLIO FOR SUPERJUNCTION MOSFETS (see page 9). ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN, EUROPE.

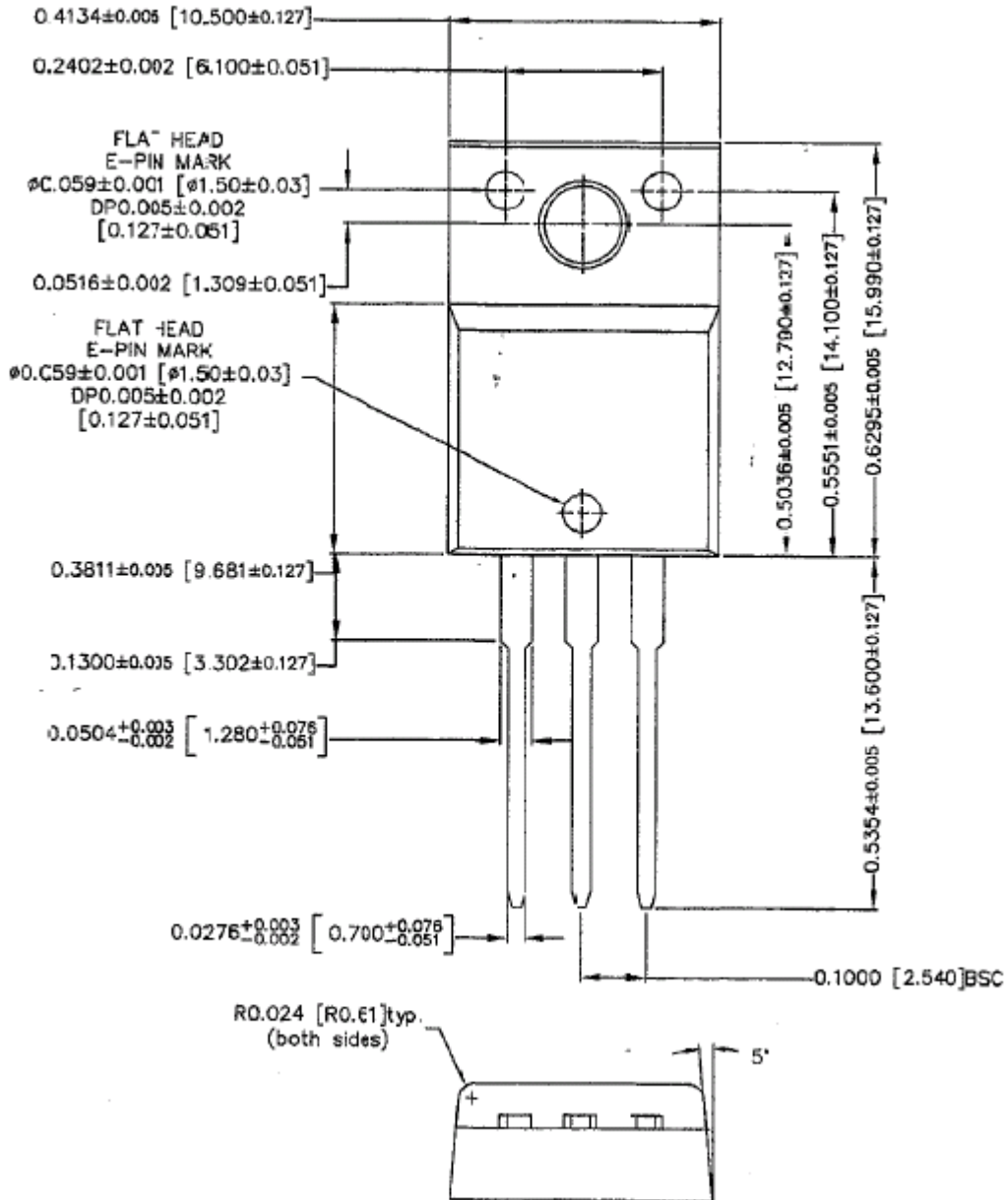
**T0220
Full-PAK
Isolated
(T0-220)**

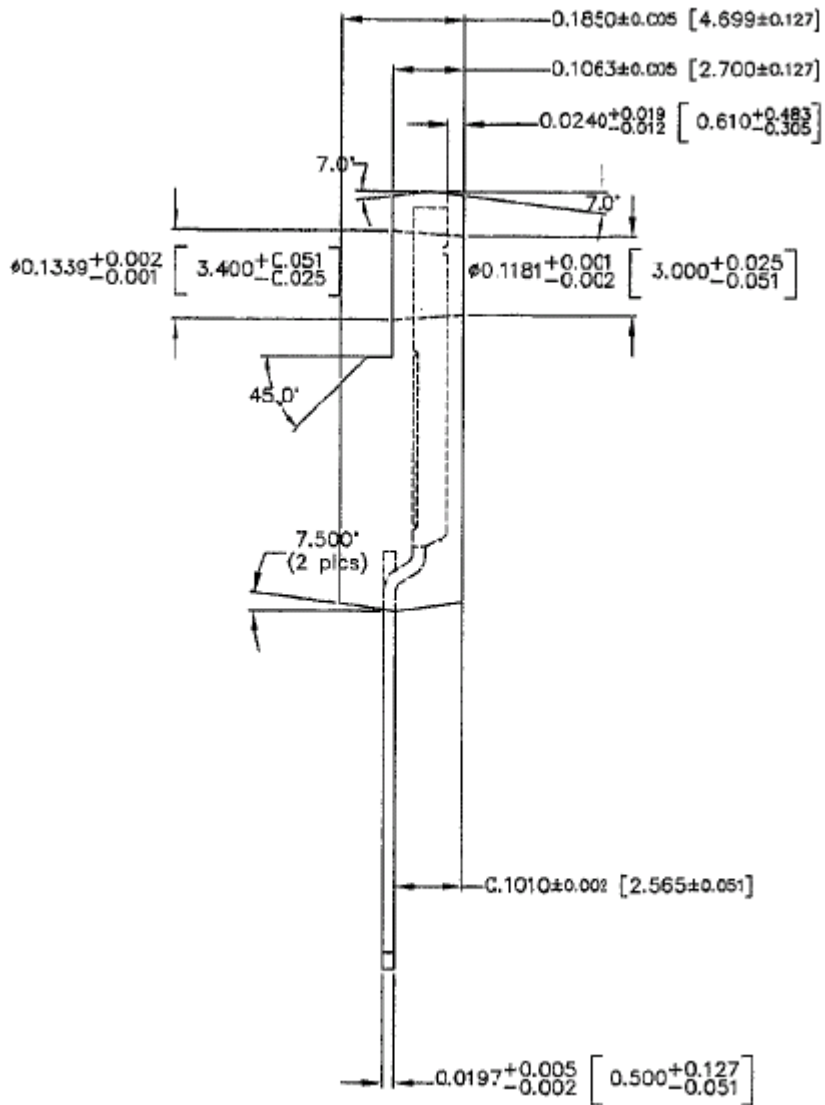
Maximum Ratings and Thermal Characteristics^b ($T_A=25^\circ\text{C}$ unless otherwise noted)

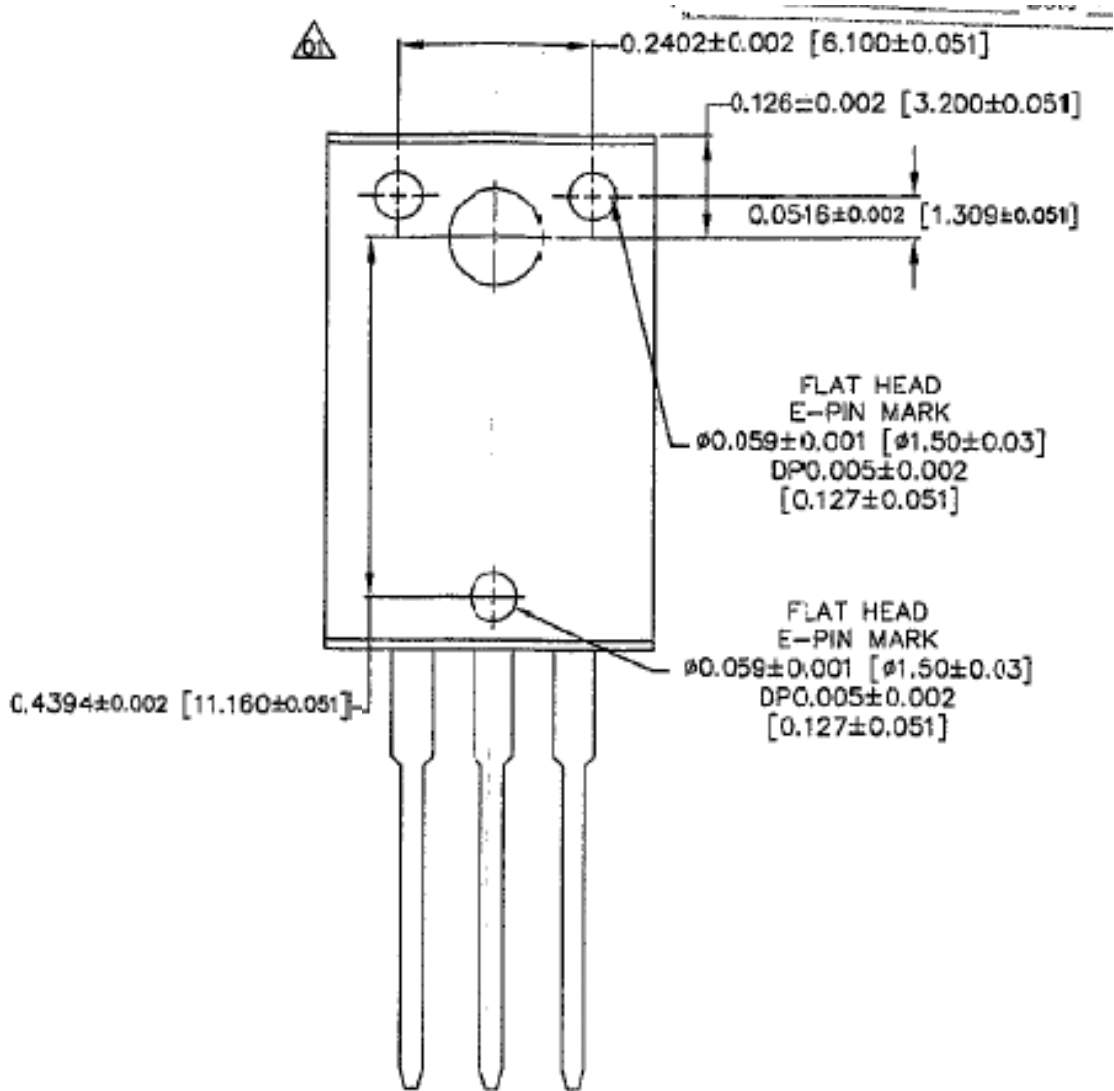
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	700	V	
Gate-Source Voltage (Static)	V_{GS}	± 20		
Gate-Source Voltage AC ($f > 1\text{Hz}$)	V_{GS}	± 30		
Drain Current	- Continuous ($T_c = 25^\circ\text{C}$)	I_D	11	A
	- Pulsed (limited by T_{jmax})	I_{DM}	33	
Repetitive Avalanche Current (limited by T_{jmax})	I_{AR}	5.5	A	
Energy in Avalanche (single pulse, $I_D = 5.5\text{A}$)	EAS	360	mJ	
Maximum Power Dissipation ($T_c = 25^\circ\text{C}$)	P_D	35	W	
Operating Junction and Storage Temperature Range	T_J, T_{sg}	-55 to 150	$^\circ\text{C}$	
dV/dt voltage slope ($V_{ds}=480\text{V}, I_D=11\text{A}, T_j = 125^\circ\text{C}$)	dV/dt	50.0	V/ns	
Thermal Resistance ^a	- Junction-to-Ambient	R_{thJA}	62	$^\circ\text{C/W}$
	- Junction-to-Case	R_{thJC}	3.50	
a When mounted on 1 inch square 2oz copper clad FR-4				
b Preliminary Data Sheet - Specifications subject to change.				

Electrical Characteristics^b (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	700	730		V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =600V, V _{GS} =0V T _J = 150°C		0.1	1	μA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =100uA	2.1	3	3.9	V
r _{DS(on)}	Drain-to-Source On-State Resistance	V _{GS} =10V, I _D =5.5A T _J = 150°C	300	350	390	mΩ
R _G	Gate Resistance	f = 1MHz,	0.2	0.5	0.7	Ω
g _{fs}	Transconductance	V _{DS} > 2*I _D *R _{DS} , I _D = 5.5A		12		S
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		1400		pF
C _{oss}	Output Capacitance			450		pF
C _{rss}	Reverse Transfer Capacitance			32		pF
t _{d(on)}	Turn-On Delay Time	V _{GS} =10V, I _D =11A, V _{DS} =380V R _G = 4Ω (External)		10		nS
t _r	Rise Time			5		nS
t _{d(off)}	Turn-Off Delay Time			67	100	nS
t _f	Fall Time			4.5	12	nS
Q _g	Total Gate Charge	V _{GS} =10V, I _D =11A, V _{DS} =480V		53		nC
Q _{gs}	Gate-to-Source Charge			9		nC
Q _{gd}	Gate-to-Drain Charge			12		nC
V _(plateau)	Gate Plateau voltage				5.5	
t _{rr}	Source-to-Drain Reverse Recovery Time	I _S =I _F , di/dt=100A/uS, V _{rr} =480V		200		nS
Q _{rr}	Reverse recovery charge			11		μC
I _{rm}	Peak reverse recovery current			70		A
V _{SD}	Diode Forward Voltage	I _S =I _F , V _{GS} =0V	0.7	1.0	1.2	V







ICEMOS SUPERJUNCTION PATENT PORTFOLIO

ICEMOS GRANTED PATENTS

US7,429,772
US7,439,178
US7,446,018
US7,579,607
US7,723,172
US7,795,045
US7,846,821
US7,944,018
US8,012,806
US8,030,133

3D SEMI PATENTS LICENSED TO ICEMOS

US7,041,560B2
US7,023,069B2
US7,364,994
US7,227,197B2
US7,304,944B2
US7,052,982B2
US7,339,252
US7,410,891
US7,439,583
US7,227,197B2
US6,635,906
US6,936,867
US7,015,104
US9,109,110
US7,271,067
US7,354,818
US7,052,982,
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.