ICEMOS TECHNOLOGY LTD

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Product Specification 47702 Issue Date 18 Nov 2005

Part Number :		**Date:**	**18 November 2005**
Customer:		**STD:**	**Y**
Customer Specification/ Reference:			

Category	*Parameter*	*Specification*	*Measurement Method*
Overall			
Wafer			
1.1	Diameter	100mm +/- 0.5	Wafer Vendor
1.2	Primary Flat Orientation	{110}+/- 1°	Wafer Vendor
1.3	Primary Flat Length	32.5mm +/-2.5	Wafer Vendor
1.4	Secondary Flat Orientation	Yes	
1.5	Thickness	478 µm +/- 6	Guaranteed by Process
1.6	Total Thickness Variation(TTV)	< 3µm	Guaranteed by Process
1.7	Bow	< 50um	ADE to ASTM F534, 20%
1.8	Warp	< 50um	ADE to ASTM F657, 20%
1.9	Edge Chips	0	Bright Light, 100%[1]
1.10	Edge Exclusion	5mm	
Handle			
Silicon			
2.1	Growth Method	CZ	Wafer Vendor
2.2	Orientation	{100}+/- 1°	Wafer Vendor
2.3	Thickness	400µm +/- 5µm	ADE, 100%
2.4	Doping type	P	Wafer Vendor
2.5	Dopant	Boron	Wafer Vendor
2.6	Resistivity	<0.02 ohm-cm	Wafer Vendor
2.7	Backside Finish	Poished with 3um oxide & lasermark ID	Guaranteed by Process
Buried			
Oxide			
3.1	Oxide Type	Thermal	
3.2	Oxide Thickness	3000 nm +/- 150nm	Nanospec centre point, 4%
3.3	Oxide formed on	Handle Wafer	

Category	*Parameter*	*Specification*	*Measurement Method*
Device			
Silicon			
4.1	Growth Method	CZ	Wafer Vendor
4.2	Orientation	{100}+/- 1°	Wafer Vendor
4.3	Nominal Thickness	75 µm	ADE, 100%
4.4	Thickness Variation	+/- 1 µm	ADE, 100% centre point
4.5	Distance to device silicon		
	edge from wafer edge	<2mm	Typical by process
4.6	Doping Type	P	Wafer Vendor
4.7	Dopant	Boron	Wafer Vendor
4.8	Resistivity	< 0.02 ohm-cm	Wafer Vendor
4.9	Voids	0	Bright Light, 100%[1]
4.10	Scratches	0	Bright Light, 100%[1]
4.11	Haze	None	Bright Light, 100%[1]
4.12	Particles	<30 @0.3um	Tencor 6220

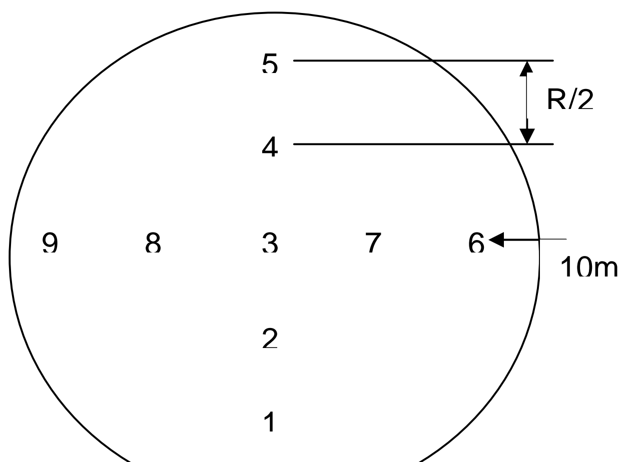
Shipping Details

Wafers per box	25 max
Packaging	Taped Polypropylene Wafer Box Empak, Ultrapak, 100mm Antistatic Double Bagging
Lot Shipment Data :	Device Silicon Thickness Handle Wafer Thickness SOI wafer thickness, TTV SOI wafer Bow/Warp

Explanatory Notes

1. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in 1.10. High intensity bright lamp inspection as per ASTM F523.

2. 9 point measurement is centre and 4 points 10mm from edge of wafer.



Approvals:	Quality:	Engineering:
	Marketing:	TRB:

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