

Part Number

Customer

Category	Parameter	Specification	Measurement Method	
OverallWafer	1.0	Diameter	150.00 +/- 0.30 mm	
	2.0	Primary Flat Orientation	{110} +/- 1 degree	Wafer Vendor
	3.0	Primary Flat Length	57.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	none	Wafer Vendor
	5.0	Overall Thickness	651.00 +/- 6.00 μ m	ADE, 100%
	6.0	Total Thickness Variation (TTV)	<3.00 μ m	Guaranteed by Process
	7.0	Bow	<40.00 μ m	ADE to ASTM F534, 100%
	8.0	Warp	<40.00 μ m	
	9.0	Edge Chips	0	Bright Light, 100% (note 2)
	10.0	Edge Exclusion	5mm	
	10.5	Bond Anneal cycle	standard anneal	Guaranteed by Process
HandleSilicon	11.0	Handle Growth Method	CZ	Wafer Vendor
	12.0	Handle Orientation	{100} +/- 1 degree	Wafer Vendor
	13.0	Handle Thickness	550.00 +/- 5.00 μ m	ADE, 100%
	14.0	Handle Doping Type	P	Wafer Vendor
	15.0	Handle Dopant	Boron	Wafer Vendor
	16.0	Handle Resistivity	1 - 5 Ohm-cm	Wafer Vendor
	17.0	Backside Finish	Lapped and etched with oxide and lasermark	Wafer Vendor
BuriedOxide	18.0	Oxide Type	Thermal	
	19.0	Oxide Thickness	10,000.00 +/- 500.00 A	Nanospec centre point, 4%
	20.0	Oxide formed on	Handle Wafer	High Anneal Temp
DeviceSilicon	21.0	Device Growth Method	CZ	Wafer Vendor
	22.0	Device Orientation	{100} +/- 1 degree	Wafer Vendor
	23.0	Nominal Thickness	100.00 +/- 1.00 μ m	FTIR, 100% 9-Pt (note3)
	24.0	Distance to device silicon edge from wafer edge	<= 2mm	Typical by Process
	25.0	Device Doping Type	P	Wafer Vendor
	26.0	Device Dopant	Boron	Wafer Vendor
	27.0	Device Resistivity	1 - 5 Ohm-cm	Wafer Vendor
	41.0	Voids	none	Wafer Vendor
	42.0	Scratches	0	Bright Light, 100% (note 2)
	43.0	Haze	none	Bright Light, 100% (note 2)

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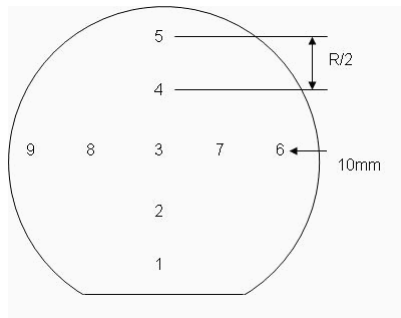
Shipping Details	Wafer per box :	Max 25
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 150.00mm Antistatic Double Bagging
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness



Explanatory Notes 1. Microscope inspection performed using microscope scan as below. 5x objective.

2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information