Influence of Cleaning on the Quality of the Bonding Interface in Direct Bonded Silicon Wafers

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Abstract. We have studied the influence of hydrophilic and hydrophobic pre-bond cleans and surface treatment of wafers on the electrical characteristics, chemical composition, crystal defects and voiding at the interface of fusion bonded silicon-on-silicon structures. Incorporation of a buried implant layer improves the electrical characteristics, but results in a deterioration of the bonding efficiency, depending strongly on the pre-join clean. The bonding yield can be improved by surface treatment of the devices and suitable modification of the cleaning process.

Introduction

Fusion bonded silicon-on-silicon (Si-Si) structures have received increasing attention in recent years as replacements for thick epitaxial (EPI) layers in high power devices, such as thyristors, insulated gate bipolar transistors and novel power devices, as well as being used in new kinds of micro-machined device [I] and semi-insulating silicon structures [2]. The material has a number of advantages, including high crystal quality, and flexibility of doping type and concentration. The bonded structures are usually fabricated by contacting two mirror-polished silicon wafers at room temperature, followed by annealing at high temperature, to form strong Si-Si or Si-O-Si bonds across the interface. One of the most important factors in determining the performance in these structures is the quality of the bonding interface. Depending on the pre-bond clean or other surface treatment, various impurities may be incorporated at the interface which can diffuse out into the active layers during the bond anneal or subsequent processing, and influence the electrical characteristics. In addition, stress- or impurity-related crystal defects, such as dislocations or slip, may occur at or near the interface, resulting, for example from the thermal break up of a thin native oxide. The presence of particle-originated voids or microvoids may also lower the quality of the interface, depending on surface roughness, particle cleaning efficiency and residual impurities.

In this work, we have studied the influence of hydrophilic and hydrophobic pre-bond cleans and surface treatment of the wafers on the interfacial properties of Si-Si structures, including electrical characteristics, chemical composition, crystal defects and voiding. In particular, we have examined the use of buried implanted layers to getter impurities at the bonding interface.

Experimental

The Si-Si bonded samples were prepared by joining polished 4" 525 /.lm thick <111 > , 3000 ohm- cm, FZ, n-type (P} silicon device wafers to <111>, 0.01 ohrn-cm, CZ, n-type (As} handle wafers using hydrophilic (ammonia/hydrogen peroxide; modified SC-l} or hydrophobic (HF last} pre-join cleans, followed by bond-annealing at 1050 or 1150°C for I h. Buried layers of dopant were fabricated at the interface by performing a blanket implant into the device surface before joining. The high-resistivity layer was then thinned to 2-100 /.lm by grinding and chemical-mechanical polishing. The Si-Si bonded interfaces were characterised using spreading resistance profile (SRP} measurements, photoluminescence (PL} (Biorad Sipher} [3], scanning acoustic microscopy (SAM}, transmission electron microscopy (TEM} and atomic force microscopy (AFM}, and by secondary ion mass spectroscopy (SIMS} on samples in which the top layer was thinned to 2-4 um.

Results and Discussion

Interfacial contamination

Figures 1 (a) and (b) compare SRP results for samples without buried dopant layers, which had an SC-I pre-bond clean, and bond anneal at 1050 and 1150°C. For the higher temperature sample, the carrier type in the n- layer inverts from n to p type over a 15um wide region next to the interface. Going further out into the top layer, the p type carrier concentration decreases, giving a I5um wide intrinsic region, becoming n type further out into the bulk. The sample annealed at 1050°C shows a much smaller effect, with only a shoulder observed in the n- layer near the interface. The results indicate that the inverted region is caused by an impurity trapped at the interface at bonding, which diffuses out into the n- layer during the high-temperature anneal. Interestingly, leaving the 1050°C sample for several months at room temperature resulted in the appearance of a similar p type region, indicating that the impurity can also diffuse slowly at low temperature. Imaging of the interface region of the 1150°C annealed sample using the PL technique revealed a high concentration of black wavy structural defects and a fairly uniform distribution of bright circular islands, as seen in Fig. 2(a).

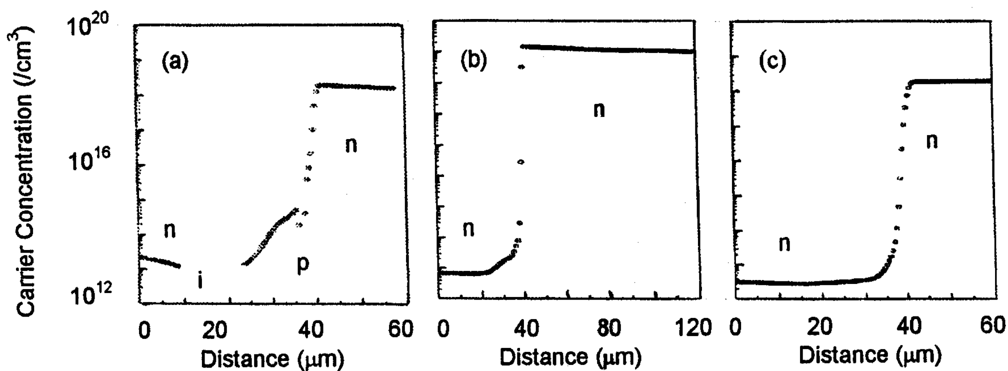

Figure 1. Spreading resistance profiles for Si-Si samples prepared using an SC-1 clean and bond anneal at (a) 1150°C and (b) 1050°C; and (c) HF last clean and bond anneal at 1150°C.

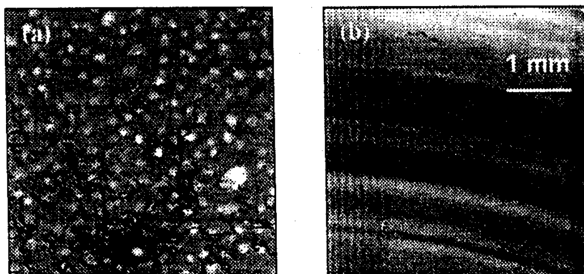

Figure 2. Photoluminescence images of interfacial defects in Si-Si samples prepared using (a) SC-1 last, and (b) HF last pre-join cleans.

Examination by TEM identified the circular regions to be islands of 6 nrn thick agglomerated oxide, separated by continuous regions of 2 nrn thick oxide. The wavy features were found to be screw dislocations in the device layer close to the interface, with associated precipitates of

copper. In contrast, the HF-last samples showed a good electrical junction at the interface (Fig. lc) and a PL image with no evidence of screw dislocations or oxygen agglomerates (Fig. 2b). SIMS across the interface indicated levels of metals such as Al and Ca of around two orders of magnitude higher for the SC-l clean, while Cu was also found, although the results showed similar levels for both cleans. Since Cu is known to diffuse readily in silicon at low temperature, it would appear to be a strong candidate for the origin of the inversion layer. In the case of the HF last clean, the interface may be gettering the Cu, as has been found previously for Au impurities at Si-Si hydrophobic interfaces [4].

We attempted to control the diffusion of impurities from the interface into the device layer of SC- 1 cleaned samples by using various gettering techniques, including oxygen precipitation in the handle wafer, polysilicon deposition, and inserting an implanted doped layer into the device at the interface. The best results were obtained with a phosphorous implanted buried layer. Figure 3(a) shows an SRP of a sample with a dose of $5e^{I5}$ /cm^2, which was bond annealed at 1150^0C . The profile is similar to the HF last sample, with no evidence of any formation of the p type inversion region. The effect was found to depend on the phosphorous concentration. For a $1e^{15}$/cm^2 dose, the region next to the interface became intrinsic (Fig. 3b), indicating some out diffusion of the impurity, while at lower doses, a p type peak again appeared. In contrast, no gettering effect was seen with As implants of similar dose, and an inverted p type region formed, similar to the unimplanted structures (Fig. 3c).

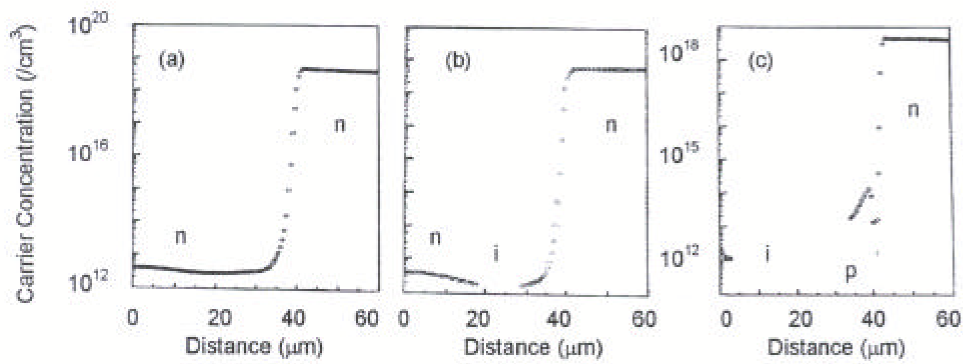

Figure 3. Spreading resistance profiles for Si-Si samples with an SC-1 clean and buried implant of (a) $5e^{15}/cm^2$ phosphorous, (b) $1e^{15}/cm^2$ phosphorous, and (c) $3e^{15}/cm^2$ arsenic.

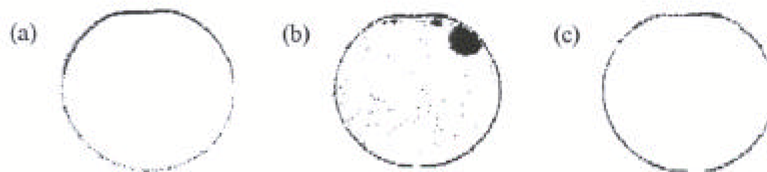

Figure 4. SAM images of bond-annealed Si-Si prepared using an SC-1 last clean: (a) unimplanted device; (b) $5e^{15}/cm^2$ P implant; (c) $5e^{15}/cm^2$ P implant with surface anneal.

Figure 5. SAM images of Si-Si with annealed As-implanted devices, using an HF last clean: (a) $5e^{13}/cm^2$ implant; (b) $2.5e^{15}/cm^2$ implant; (c) $2.5e^{15}/cm^2$ implant with modified clean.

Bonding efficiency

The introduction of a buried implant caused a significant deterioration in bonding quality, in terms of microvoids and particle-originated voids, and this was found to be strongly influenced by the wafer surface treatment and cleaning process used. AFM analysis showed that implanting an As or P

layer resulted in roughening of the silicon surface by a factor of around two, the effect increasing with both increasing implantation energy and dose. The roughening caused a reduction in the speed of the bonding wave, and associated increase in particle-voiding and microvoiding after the bond anneal. This effect depended strongly on the pre-bond clean. Figure 4 shows SAM images of unimplanted and P-implanted samples, joined using an SC-1 last clean. The unimplanted sample is completely void-free, while the implanted wafer shows a high degree of microvoiding as well as larger particle-related voids. However, by using a surface annealing treatment on the implanted wafer, to reduce the amount of crystalline damage at the surface, a good bonding wave was achieved, resulting in a void-free bond, as shown in Fig. 4(c). Similar results were obtained with As implants. In contrast, with the HF last clean, a spontaneous bonding wave did not occur for equivalent-dose implanted wafers. After surface-annealing, a slow bonding wave was obtained, but the bond-annealed samples had significant voiding, with the yield strongly dependent on the implant dose. This is seen in Figs. 5 (a) and (b), which show a much higher degree of particle-voiding and microvoiding for the higher-implant sample. It appears from the results that the native oxide present after the SC-1 clean must act as a buffer to reduce the influence of implant-related surface effects, creating a stronger interaction between the wafers at joining, and resulting in a reduction in particle- originated interfacial voids. In addition, the TEM results show that at the annealing temperature used, the native oxide can flow along the bonding interface, which may also help to eliminate microvioiding. Without this native oxide, as in the case of the hydrophobic clean, a greater sensitivity to the wafer surface is observed. However, by modifying the pre-bond cleaning process to reduce the amount of surface roughening occurring during the clean, we were able to achieve hydrophobic void-free bonding, even in the presence of a high-dose implant, as shown in Fig. 5(c).

Conclusions

We have found that a hydrophilic SC-1 pre-join clean results in the incorporation of impurities at the bonding interface of Si-Si structures, which can diffuse out at low temperature, causing growth of crystalline defects near the interface and deterioration of the electrical properties in low-resistivity device layers. The impurity can be gettered using a buried layer of phosphorous at the interface, formed by implanting a high dose of phosphorous into the device surface before

bonding. In contrast, a hydrophobic HF last clean gives good interfacial and bulk electrical properties, together with significantly reduced defect formation. The attainment of high bonding efficiency in terms of voiding is more difficult with a hydrophobic clean, particularly when using implanted devices, but has been achieved by reducing the amount of roughening of the device surface before bonding.

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