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Bonded and Trenched SOI with Buried Silicide Layers

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This paper presents for the first time a commercially viable bonded and trenched SOI technology incorporating a buried CVD tungsten silicide layer. The CVD WSi layer was deposited 11nto the device wafer prior to bond. A trench etch process was developed which allowed the patterning of the thinned SOI silicon layer and the underlying silicide in a single step with high selectivity and no undercut. Fully processed bonded, thinned, trenched, filled and planarized SOI structures are demonstrated and shown to be stable at 1150C.

Introduction

Metal silicides are widely used in CMOS processing to lower the resistance of polysilicon gates. This combination of polysilicon and silicide is commonly referred to as a polycide. Tungsten silicide is the most commonly used silicide for this application. This is because tungsten silicide can be easily deposited in uniform, low stress, high purity layers which are thermally stable, easy to pattern and are compatible with all high temperature IC processing [1]. In this paper, this well established silicide technology is used to lower the resistance of a buried layer within an SOI structure. This is accomplished by depositing a CVD tungsten silicide layer onto the device wafer prior to bond.

Buried layers are widely used in IC processes which incorporate transistors with vertical current flow. This includes most bipolar transistors as well as power MOS transistors. The buried layer is used to lower the resistance of the collector/drain of the device and thus improve its speed and power handling capability. In Smart Power applications, the resistance of this buried layer is the single most important limitation on power handling capability .In high performance analog IC applications the switching speed is limited by the buried layer resistance which forms an RC time constant with the substrate.

In conventional epitaxial technology I the resistivity of the buried layer is limited to about 2Ohm./sq. This is because high quality single crystal material can not be grown on surfaces with a doping concentrations in excess of lEl9cm^{-3}. This limitation can be overcome in wafer bonding by ion implanting the device wafer prior to bonding. In this case, no limitation on doping exists and buried layers of lO.0./sq. can be achieved. However, this factor of two reduction is not sufficient for many applications where even higher conductivity is required. Achieving higher conductivity requires the use of a refractory metal silicide.

Experimental

Silicide Formation

Buried silicide layers in SOI structures have been previously reported using direct reaction silicides [2,3,4]. In these cases the silicides used were titanium silicide ($TiSi_2$), tantalum silicide ($TaSi_2$) and cobalt silicide ($CoSi_2$). The direct reaction process heats a pure metal in contact with a silicon wafer to form a metal silicide layer. In the case of wafer bonding, the reaction was used not only to form the silicide layer but also as a "glue" to bond the wafers together .

Direct reaction silicide formation results in a highly stressed silicide layer which makes it undesirable for buried layer applications. The high stress is a result of the significant volume expansion that occurs during the silicide reaction. This highly stressed layer limits the silicide film thickness, or conductivity, and the maximum temperature of operation. As an example, the buried TaSi2 layer reported above limited the film thickness to 0.l2um and the maximum temperature to l000C. A second limitation of this technique concerns the reliability of the bonded interface. The bonding of silicon to silicon dioxide is now well established, but very little is known about the bonding strength of direct reaction silicide bonds.

This work focuses on the use of the industry standard CVD tungsten silicide (WSi_2) as the buried silicide layer using a silicon to silicon dioxide bonding interface. CVD tungsten silicide can be deposited in a number of commercial systems [5,6] from the reaction of tungsten hexaflouride and silane. WSi films are high purity, uniform, low stress, high conductivity, of controlled stoichiometry and are of proven compatibility with IC processing. These films are know to be stable at I200C and with a conductivity of 30micro ohm/cm, they offer a significant improvement over ion implanted layers [I].

The WSi was deposited in a commercially available reactor onto an undoped device wafer with a stoichiometry of $WSi_{2.4-2.6}$ to prevent any reaction of the silicide with the underlying substrate. All films were deposited to a thickness of 0.3 urn. These films had highly reflective mirror like surfaces. The WSi films were bonded as- deposited or after post deposition, pre-bond anneals of 900,1000 and 1100C anneals in nitrogen.

Structure

To insure maximum compatibility with subsequent IC processing, the well established $Si-SiO_2$ bond interface was used. Two different structures were examined, both of which offer potential advantages [Fig lA and B].

The structure shown in Fig lA is the conventional polycide structure. In this case the device wafer is covered with a layer of WSi followed by a layer of LPCVD poly silicon. This polysilicon layer is then bonded to an oxidized handle wafer .

The structure shown in Fig IB uses only the silicide layer. The device wafer is covered with a layer of WSi followed by a layer of LPCVD TEOS oxide. The TEOS oxide layer is bonded to a bare silicon handle wafer .

Bonding

All wafers were bonded using the same technique. The wafers were first cleaned in a dilute megasonic RCA clean [7], rinsed in Dl, spun dry and joined. After joining, the wafers were inspected in m prior to bonding. Wafer were bonded at temperatures ranging from 800 to 1100C. After bonding the wafer were inspected with a scanning acoustic microscope (SAM) for voids. Cross sectional SEM examination of the bonded interface was also done on selected wafers.

Thinning

After bonding, the wafer were thinned to SOI layers of l0um and 5um with a tolerance of +1- 0.5.um using conventional mechanical thinning technology. After thinning the wafers were reannealled from 900C to 1150C to determine the stability of the films. Again, SAT inspection was done on all wafers and cross-sectional SEM examination of the bonded interface was also done on selected wafers

Trench Etch and Fill

After SOI formation, an LPCVD TEOS hardmask was deposited. This was patterned in RIE using photo resist as a mask. The top SOI structure was then etched in an HBr chemistry .The same conditions were used for etching the entire stack which in one case was the single crystal silicon and the WSi and in the other case was the single crystal silicon layer, the WSi layer and the underlying polysilicon layer. After selective removal of the TEOS hardmask, the trench was filled with a sidewall oxide followed by an LPCVD polysilicon fill. The trenched wafers were then planarized using CMP .After trench planarization, the wafers were coated with an LPCVD TEOS layer. Cross sectional SEM examination was done on selected wafers of the as- etched trench and the filled and planarized trench.

Post Trench Processing

The finished bonded and trenched SOI wafers were then oxidized at 1150C in steam for 240 mins to simulate the subsequent lC processing. Cross sectional SEM examination was done on selected wafers.

Results

Bonding

In all cases the bonding was spontaneous. The wave velocity was 1.2 cm/sec for the polysilicon coated silicide and the 1.0 cm/sec for the undoped TEOS layer. In all cases the wafers were voidless under IR examination.

The pre-bond annealing of the WSi layer after deposition and prior to LPCVD poly or TEOS had no impact on the joining of the wafers. All wafers including the as-deposited silicide layers joined voidlessly.

After annealing, all bonded wafers were voidless as examined by SAM. Fig 2 is an SAM image of a typical bonded wafer showing voidless bonding. No influence was seen by either pre-bond annealing of the silicide or of bonding temperature. As-deposited silicide bonded at 800C appear identical to wafers with a 1100C pre-bond anneal and an 1100C bond. Cross sectional SEM's of the bonded interface show a uniform silicide layer 0.3um thick with no shrinkage, agglomeration or other defects.

Thinning

The excellent bond strength was demonstrated by the ability to thin wafers bonded at BOOC without delamination, fractures or chipping due to poor bond strength. After thinning, no sign of delamination, voids or other defects were detected on any wafer .

Figs 3A and 3B are cross-sectional SEMs of an SOI structure before and after an 1150C steam oxidation for 240 min. The WSi layer remains intact and unchanged by this heat treatment. Lower temperature and shorter time oxidations showed similar results.

Trench Etch and Fill

The trench etch process successfully patterned the buried silicide or silicide/poly structure with near vertical positively tapered walls. Fig 4A is a cross sectional SEM of an as-etched trench. As shown, the etch process has no undercut of the silicide or the underlying polysilicon layer .

Even trenches that were intentionally over etched [Fig 4B] by as much as 25% showed no lateral attack of the silicide layer .All wafers etched identically independent of prior thermal treatment.

Post Trench Processing

Cross sectional SEM examination of wafers that were thermally treated after etch and fill show no effect on the silicide layer. In all cases the WSi remained a continuous defect free layer .Fig 5 is an cross sectional SEM of a filled trench that was oxidized at 1150C for 240 min in steam prior to trench etch and then a second 1150C, 240 min steam oxidation after trench etch and fill. Again, no degradation of the buried silicide layer was observed.

Discussion

These results show that WSi can be incorporated into a commercially viable SOI structure while achieving conductivities that are higher than can be achieved by ion implanted buried layers. The structures tested were processed through the front end of a trenched SOI wafer process without degradation of any kind. In addition, post trench thermal cycling that is consistent with a complete process again showed no degradation of the WSi layer or any other layer(s) within the SOI structure.

The WSi directly in contact with the lightly doped single crystal silicon layer will form a Schottky barrier contact. To achieve an ohmic contact, sufficient doping must be introduced at the interface to lower the Schottky barrier height. The resistivity of this doping is unimportant as all conductivity will be provided by the silicide layer . This doping can be provide by ion implantation or in the case of the poly silicon covered WSi layer , by in-situ doping.

While the silicide offers a unique advantage for applications that demand very high conductivity buried layer, it also offers advantages for more conventional applications in which a very high conductivity buried layers is not required. For any given conductivity, the silicide layer will be considerably thinner than a conventionally doped buried layer .As a result, the trench depth of the silicided wafer will be reduced over that of the conventional doped buried layer wafer. This reduction in trench depth in turn reduces other parameters such as etch time, trench width and hard mask oxide thickness all of which reduce die cost. Depending on the application, this cost savings could more than pay for the additional cost of the blanket silicide layer .In this case a higher conductivity buried layer could be enjoyed while simultaneously lowering process cost.

Buried silicide layers may also be of use in thick film SOl CMOS processes to improve gate oxide quality while simultaneously reducing latch-up. The silicide single crystal interface will act as a gettering site which will trap heavy metals or other crystallographic defects keeping the SOl layer defect free. This will improve gate oxide quality without requiring surface gettering [8] or trench sidewall gettering [9] which consume valuable space and lower circuit density. In addition, if the silicide layer is doped to achieve an ohmic contact with the SOI layer it will provide a low resistivity path between the parasitic bipolar base-emitter junction preventing latch-up.

In addition to the IC applications, buried silicide layers could have important applications in micromachining and integrated IR optics.

Conclusion

Two techniques have been demonstrated for bonding CVD WSi coated device wafers to form buried silicide SOI substrates that are compatible with IC fabrication. The bonding was shown to be voidless and independent of any pre-bond annealing of the WSi. Bonded wafers were thinned and further oxidized at 1150C for extended periods without degradation of any kind. The ability to trench etch both structures without undercut was demonstrated. Fully processed bonded, trenched and planarized SOI wafers were further subject to heat treatments at 1150C, again without degradation. Thus a fully dielectrically isolated substrate process incorporating a buried silicide layer has been successfully demonstrated.

References

1.S.P. Murarka, "Silicides for VLSI Applications", Academic Press, New York, 1983.

2. D. Nayak, A. Reisman, I. Turlik, "Metal-to-Metal Bonding Using an Oxidizing Ambient Atmosphere", ECS, vol135, No 4, pp1023-1025, 1988

3. A. Fukuroda, T. Sugh, Y. Arimoto and T. Ito, "Si Wafer Bonding with Ta Silicide Formation", Jpn JAP, Vol 30, No. 10A, Oct 91, pp1693-1695

4. K. Ljungberg, A. Soderbarg, G. Thungstrom, S. PettersSon, "Buried Silicide Layers in Silicon, Using Wafer Bonding with Cobalt as Interficial Layer", ECS, vol. 93-1 Abstract 830, May 1993

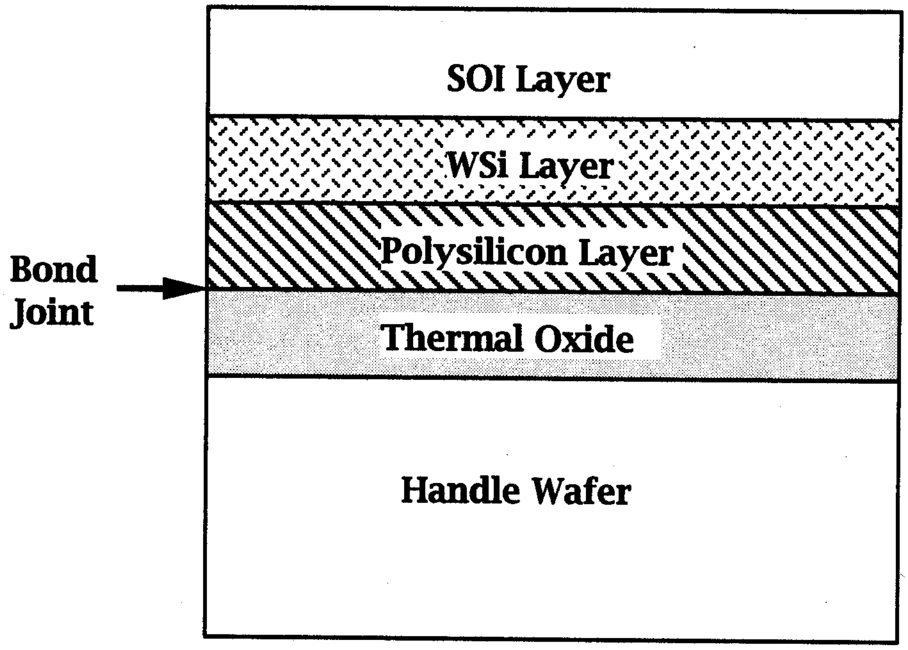
5. Novellus Systems, San Jose,

6. Ca Genus, San Jose, CA

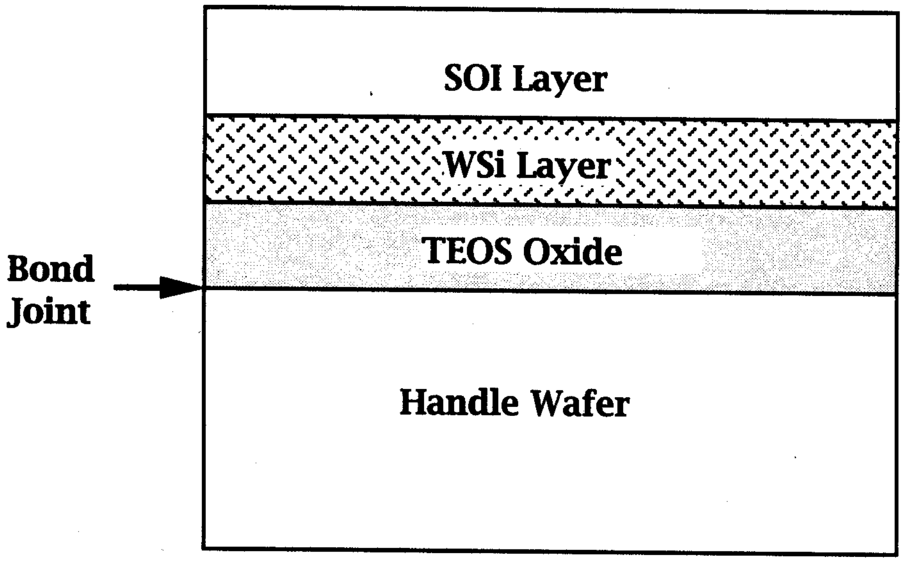
7. M. Itano, F. Kern, M. Miyashits, T. Ohmi, "Particle Removal from Silicon Wafer

Surface in Wet Cleaning Process", IEEE Semi Manufacturing, Vol 6 No.3, Aug 93

8. H.D. Chiou, F. Seccod'Aragona, E. Strickland, "Gettering of Bonded SOI Layers", ECS Extended Abstracts, Vol 92-1, Abstract 194, pp 325-326, May '92
9. K. Yallup, "Analog CMOS Circuits on Thick Film SOI', Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, ECS, vol 93-96, ppl17

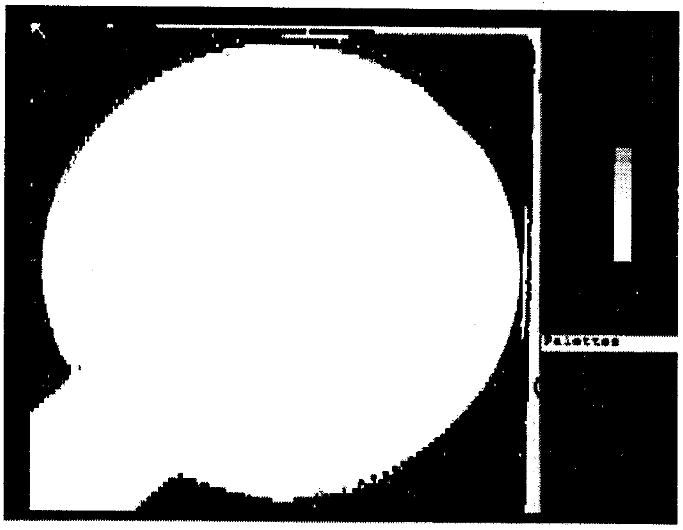


Polycide Structure
Fig 1A

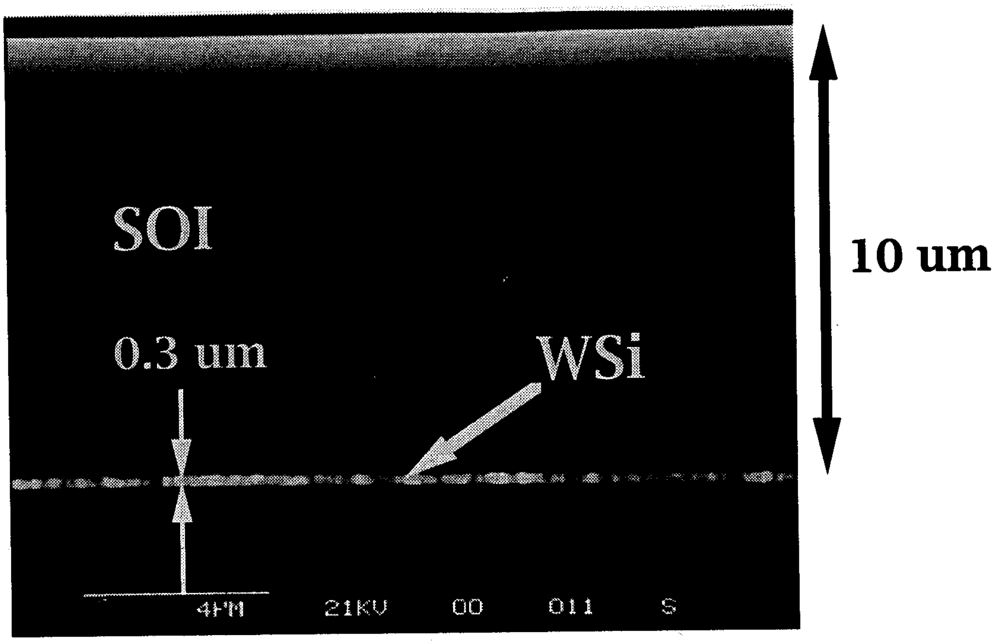


Silicide Structure
Fig 1B

Scanning Acoustic Micrograph of
Tungsten Silicide - TEOS bonded wafer
Fig 2A

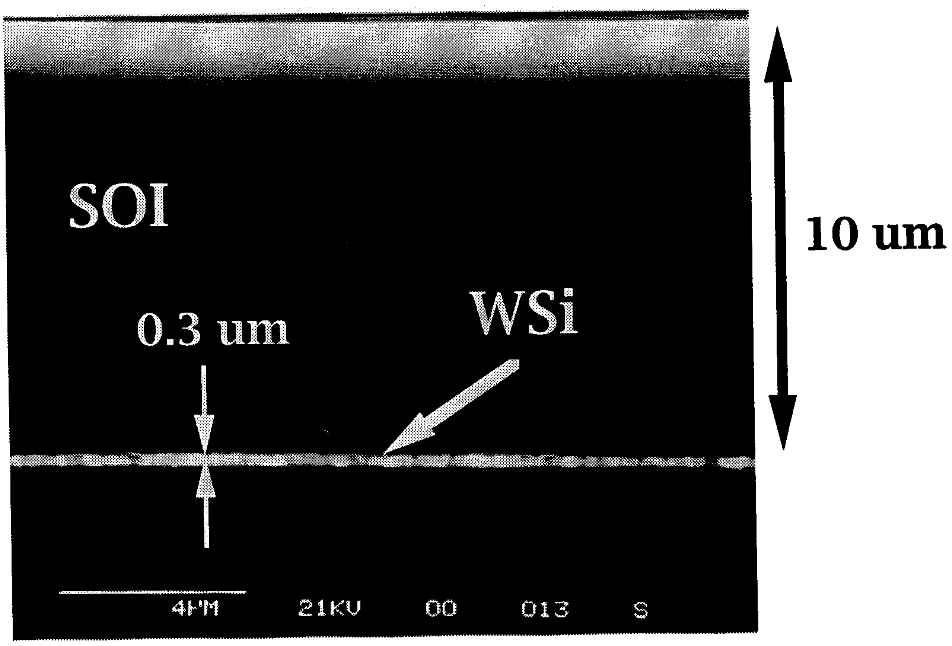


Scanning Acoustic Micrograph of
Tungsten Silicide - Polysilicon
bonded wafer
Fig 2B



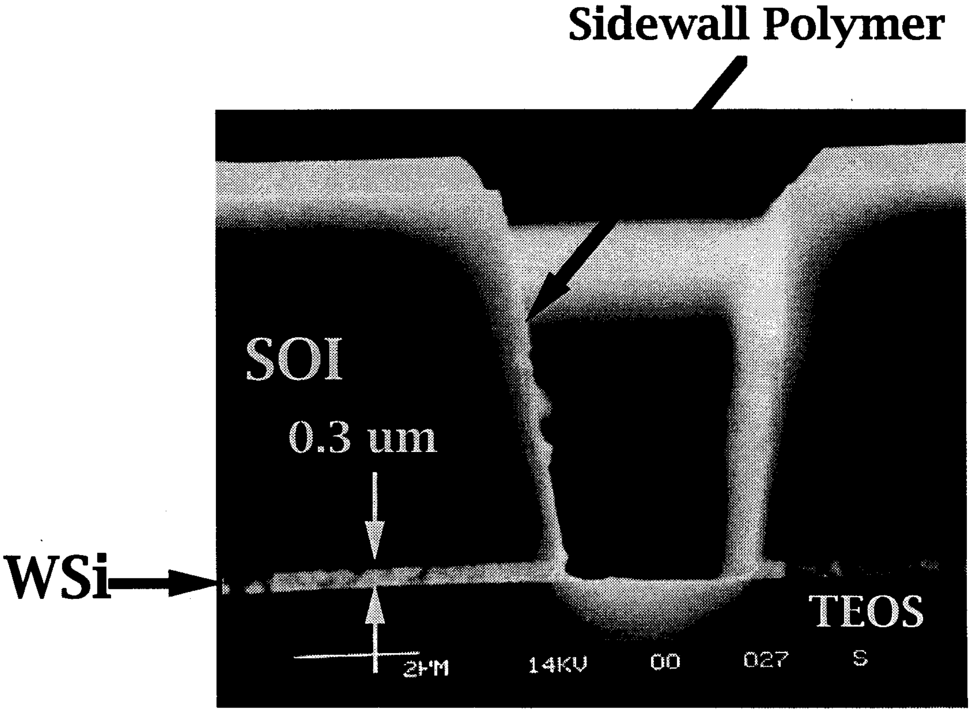
As Bonded at 1100C

Fig 3A

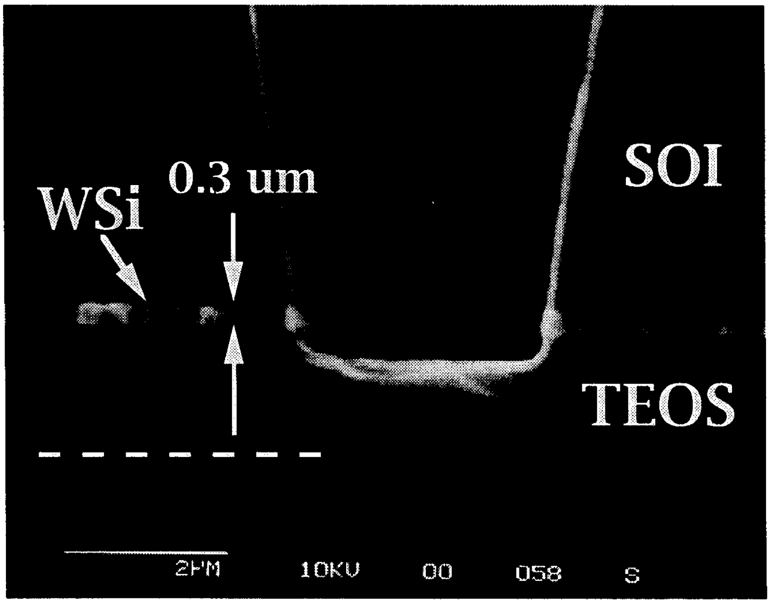


After 1150C 240 min Anneal

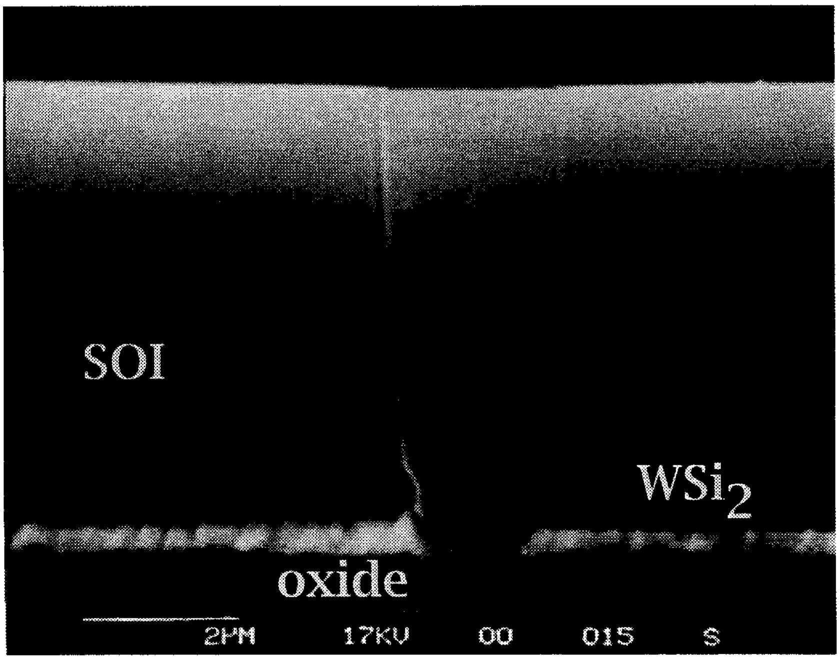
Fig 3B



As Trench Etched
Fig 4A



25% Over Etch
Fig 4B



Refilled Trench in Buried Silicide SOI wafer
Fig 5