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Material Effects on Stress-Induced Defect Generation in Trenched Silicon-on-Insulator Structures

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We have investigated the influence of the material properties of the silicon device layer on the generation of defects, and in particular slip dislocations, in trenched and refilled fusion-bonded silicon-on-insulator structures. A strong dependence of the ease of slip generation on the type of dopant species was observed, with the samples falling into three basic categories; heavily boron-doped silicon showed ready slip generation, arsenic and antimony-doped material was fairly resistant to slip, while silicon moderately or lightly doped with phosphorous or boron gave intermediate behavior. The observed behavior appears to be controlled by differences in the dislocation generation mechanism rather than by dislocation mobility. The introduction of an implanted buried layer at the bonding interface was found to result in an increase in slip generation in the silicon, again with a variation according to the dopant species. Here, the greatest slip occurred for both boron and antimony-implanted samples. The weakening of the implanted material may be related to the presence of a band of precipitates observed in the silicon near the bonding interface.
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Fusion bonded silicon-on-insulator (SOI) is becoming an increasingly important commercial substrate for the fabrication of electronic devices such as bipolar and high-voltage structures.[1,2] The buried oxide (BOX) incorporated at the bonding interface electrically isolates the top silicon device layer from the thick substrate handle layer, so that by trenching through the top layer to the BOX, and then lining the trench sidewalls with silicon oxide, electrically isolated tubs of silicon are formed, on which the devices can be fabricated. Advantages of these structures over conventional silicon substrates include reduced leakage currents and parasitic capacitances, reduced power consumption, faster switching speeds, high quality and versatility of the silicon layer type, and die shrinkage. While some SOI technologies, such as low-power complementary metal oxide semiconductor (CMOS), are now relatively mature, the utilization of SOI for high-voltage applications has been initially slower, but is rapidly gaining increasing attention, with potential applications in a wide range of areas such as telecommunications, displays, and smart power.[3,4]

A major problem in applying the trench-isolation technique to high-voltage structures is that the thickness of the sidewall oxide must be increased to give sufficient breakdown voltage. This leads to an increasing level of tensile stress exerted by the oxide on the silicon sidewall, which peaks close to the bottom corner of the trench, eventually leading to the generation of slip dislocations when the stress exceeds the yield strength of the material.[4,5] This usually occurs during thermal cycling of the structures at high temperature, and is probably the result of the difference in thermal expansion coefficient between the oxide and silicon. The degree of stress increases with increasing oxide thickness and decreasing tub size. An understanding of the effect of the silicon material properties on slip propagation is therefore important to achieving the aims of both reducing the die size and increasing the obtainable trench isolation breakdown voltage.

The object of this work was to investigate the influence of the material properties of the SOI device layer silicon on the generation of slip dislocations in this layer at filled trenches. In particular, we have varied the type and concentration of dopant species in the material and the crystallographic orientation. In addition to grown-in dopants included during the crystal pulling process, we have also examined the effect of incorporating various dopant species as implanted buried layers into the silicon material on the degree of generation of the slip dislocations.

Experimental

Starting device materials for the SOI layer were polished 4 in. diam silicon Czochralski (CZ) and float zone (FZ) wafers with various grown-in dopant species, dopant concentrations, and crystal orientation, as summarized in Table I. For the implant-dependence study, SOI with buried implanted layers at the bonding interface were prepared by blanket-implanting 3-5 Ωcm phosphorous-doped polished (100) CZ silicon device wafers, before bonding, with $5 \times 10^{15}/cm^2$ doses of ions at 80 keV. This resulted in a layer with a dopant concentration of about 5×10^{19} atoms/cm^3 in the device close to the bonding interface, after the final stage of sample processing. The handle material was 3-5 Ωcm phosphorous-doped polished CZ silicon with (100) crystal orientation. A 1.0 μm thick thermal oxide layer was grown on the handle wafers before bonding, which formed the BOX in the SOI wafer. The fabrication process of the bonded SOI wafers is illustrated in Fig. 1. The device and handle wafers were joined at room temperature following a modified RCA clean, and then bond annealed at 1050°C. The device layer was then thinned to 20 μm by grinding and chemical mechanical polishing, patterned using standard photolithographic techniques, and 3 μm wide trenches etched to the buried oxide using an inductively coupled plasma etching method.[6] The angle between the trench sidewall and the surface plane was close to 90°.

Slip dislocation generation was examined by refilling the trenches and thermally stressing the samples by annealing at high temperature. The full refill process consisted of first lining the trenches with a thick layer of low-pressure chemical vapor deposited (LPCVD) tetraethoxysilane (TEOS) oxide deposited at 700°C, then filling the centers with LPCVD polysilicon at 620°C, planarizing the polysilicon, capping the trench top with a further LPCVD oxide layer, and annealing at 1050°C for 1 h in nitrogen at two stages of the refill process (see Fig. 2). A schematic diagram of the complete refilled structure is shown in Fig. 3. The thermal annealing resulted in densification and shrinkage of the LPCVD oxide films by around 5%. The degree of generated slip during the refill was analyzed by inspecting the SOI surface using phase-sensitive Nomarski optical microscopy, and at the end of the process by Secco etching of cross sections and examination by scanning electron microscopy (SEM). Four to eight samples were processed in each group of wafers. The degree of slip was estimated for each wafer as a percentage of die affected by slip, measured along two lines across the entire wafer

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Table I. Properties of device material used for SOI fabrication, oxidation-induced defect densities in the SOI layers, and results of slip inspections in trenched samples with a 1.1 μm thick oxide liner.

	Material properties				Degree of slip (%)				
Dopant	Concentration (atoms/cm^3)	Resistivity (Ωcm)	Growth type	Orientation	Liner dep.	Liner dens.	Final dens.	Defect density ($10^3/cm^2$)	Oxygen content (10^{17}atoms/cm^3)
B	9.0×10^{18}	0.01	CZ	(100)	96	100	100	900	8.1
B	9.5×10^{14}	14	CZ	(100)	0	13	39	2.5	5.0
B	3.8×10^{14}	35	CZ	(100)	0	38	69		2.0
P	8.0×10^{16}	0.1	FZ	(111)	4	69	75	0.5	<0.4
P	1.1×10^{15}	4	FZ	(100)	0	60	78	1.1	<0.4
P	1.4×10^{12}	3000	FZ	(111)	7	42	53	2.2	<0.4
As	8.0×10^{18}	0.007	CZ	(100)	0	9	20	<0.5	8.1
As	4.5×10^{18}	0.01	CZ	(111)	0	4	12	2.5	5.6
Sb	1.8×10^{17}	0.06	CZ	(100)	0	5	10	2.2	6.1
Sb	2.8×10^{17}	0.04	CZ	(111)	0	0	0	6.8	5.7

diameter, perpendicular and parallel to the flat, bisecting at the wafer center (one affected tub in a die constituted a positive count). The total number of die along these lines was 81, and the dimension of each die was about 1 mm square. To allow for an observed wafer-to-wafer variation, the slip was taken as the average value of all the wafers in a given group.

Oxygen concentrations in the SOI layers were measured by secondary-ion mass spectroscopy (SIMS) at DERA (system background level = 3-4 $\times 10^{16}$ atoms/cm^3), calibrated by reference to O implants in Si. These values were adjusted to the new ASTM infrared calibration using a 26% downscaling factor obtained by comparing Fourier transform infrared (FTIR) and SIMS measurements from two prime Si wafers.[7] Transmission electron microscopy (TEM) was carried out at DERA.

To measure the minority carrier lifetime and study oxygen precipitation behavior in the SOI device wafers, untrenched SOI were thermally oxidized in wet oxygen at 1050°C, to grow a 500 nm thick oxide layer. The minority carrier lifetime was measured by a surface charge analysis (SCA)[8] nine-point mapping method, using a Semitest model SCA2500 instrument. The nine points were located across and along the wafer surface. The SCA signal was generated by a short 560 nm wavelength illumination that ensured shallow penetration depth (1.8 μm) of the incident light and enabled carrier lifetime measurement in the near-surface region of the SOI layer. At this penetration depth almost all carriers were photogenerated within the surface depletion layer and all minority carriers were swept by the electric field toward the surface. This made the SCA measurements insensitive to diffusion effects and provided effective separation of the surface from the bulk related effects.

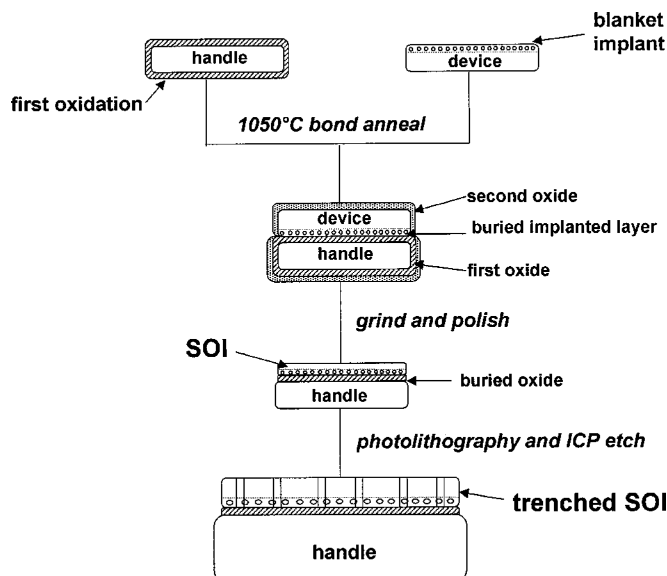

Figure 1. Schematic diagram of the bonding procedure.

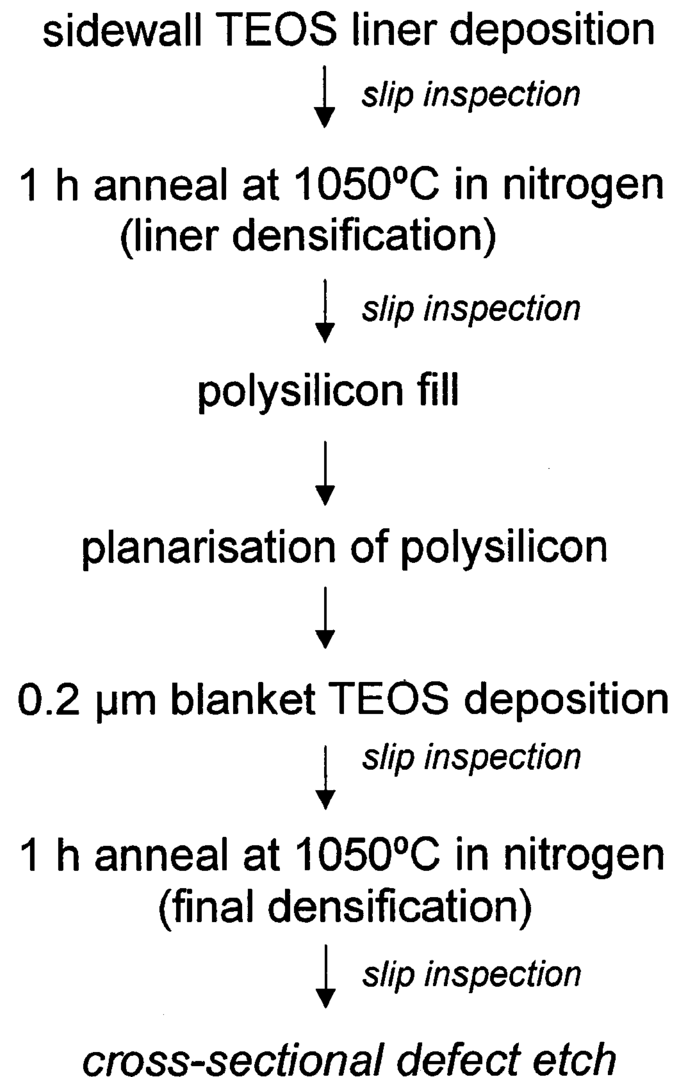

Figure 2. Schematic diagram of the trench fill, thermal annealing, and inspection sequence.

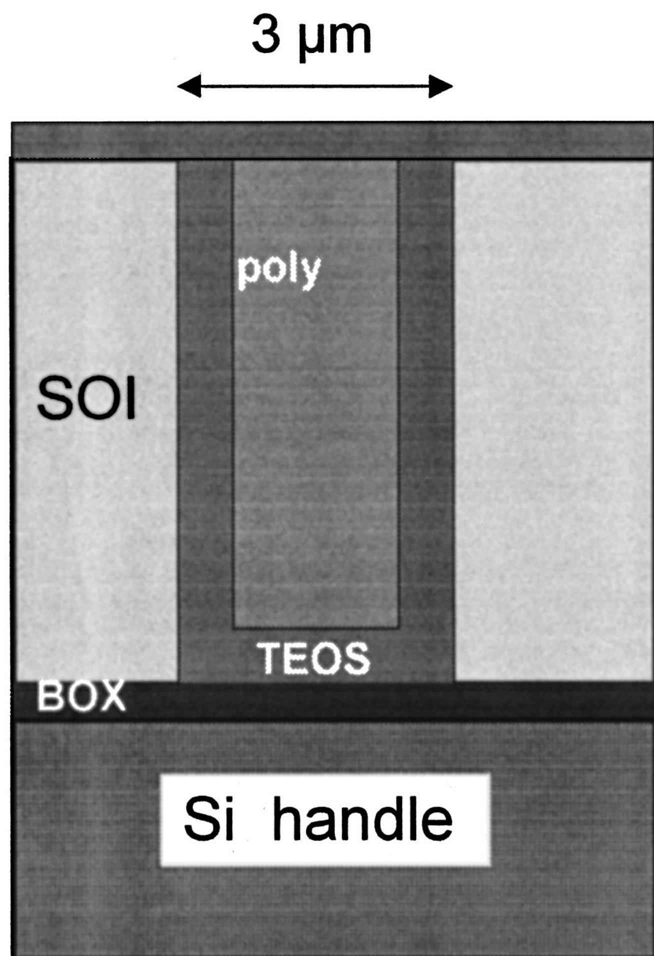

Figure 3. Schematic diagram of the completed trench-filled SOI structure.

After SCA analysis the wafers were stripped of the surface oxide, immersed in Secco etch[9] solution for 1.5 min and subsequently cleaned. Examination of the etched surface by optical microscopy revealed the nature and distribution of crystalline imperfections present, and defect densities were estimated by counting the number of defects in calibrated optical microcrographs. The defect density could not be determined by optical observations when the density was lower than $5 \times 10^2/cm^2$.

Results and Discussion

Effect of grown-in silicon dopants.—Results of slip inspections at the processing stages of post oxide liner deposition, post liner densification and post final oxide densification are listed in Table I. We observed a strong dependence of the ease of slip generation on the type of dopant species in the silicon device material. In the heavily boron-doped samples, a high level of slip was found immediately after deposition of the CVD oxide liner, as seen in the Nomarski micrograph of Fig. 4a. Similar to previous studies,[5] the slip emanates from high-stress regions near the bottom corners of the trenches, propagates along the Si (111) plane, and is seen at the surface as lines running parallel to the trenches. This was verified by Secco etching cross sections of the wafers, which showed an angle of 50-54° between the slip line and the wafer surface, which is similar to the angle between the (100) and (111) crystallographic planes. In contrast, the other material groups showed little or no slip at the liner deposition stage, but the degree of slip was then seen to increase with each high-temperature annealing cycle. For example, the degree of slip in the slightly doped (1×10^{12} atoms/cm^3) phosphorous samples increased from 7% at liner deposition, to 42% at liner densification, to 53% after the final densification. The arsenic and antimony wafers had more resistance to slip, with one of the antimony groups remaining entirely slip-free through the complete trench refill and thermal cycling [see Fig. 4b]. Typical SEMs of Secco-etched cross sections for heavily and lightly boron-doped and for antimony-doped samples, taken after the final thermal processing step, are shown in Fig. 5, and confirm the results of the optical inspections. In the heavily boron-doped sample, extensive slip is

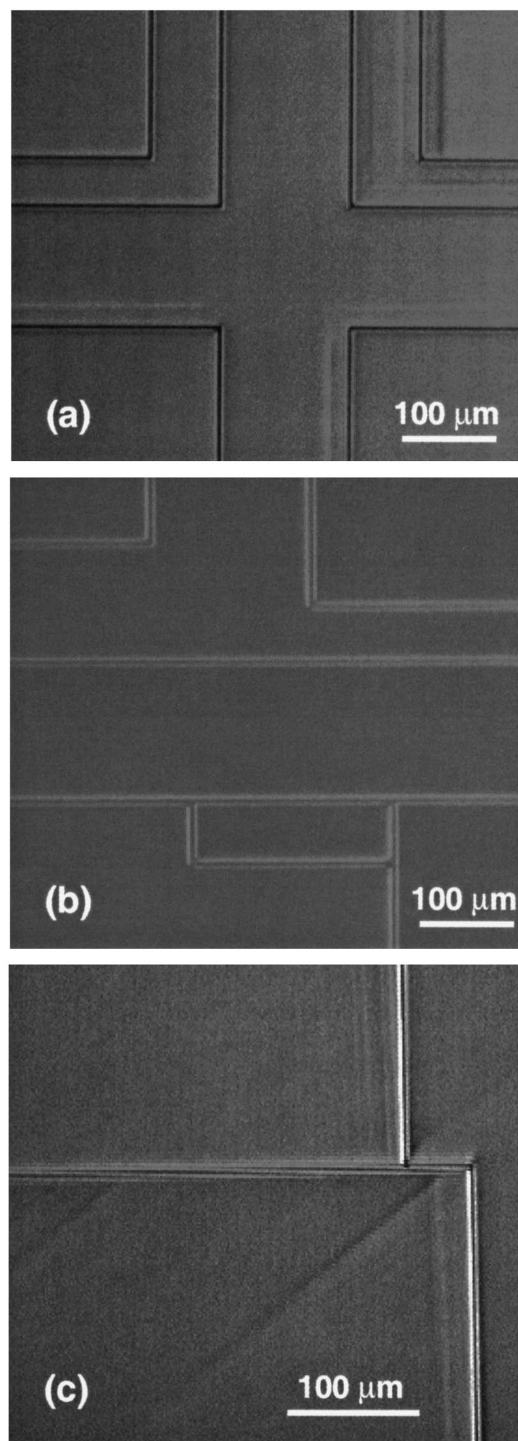

Figure 4. Plan-view Nomarski images showing slip lines at the surfaces of trenched and refilled SOI samples prepared using (a) 0.01 Ωcm B-doped (100), (b) 0.04 Ωcm Sb-doped (111), and (c) 3000 Ωcm P-doped (111) silicon.

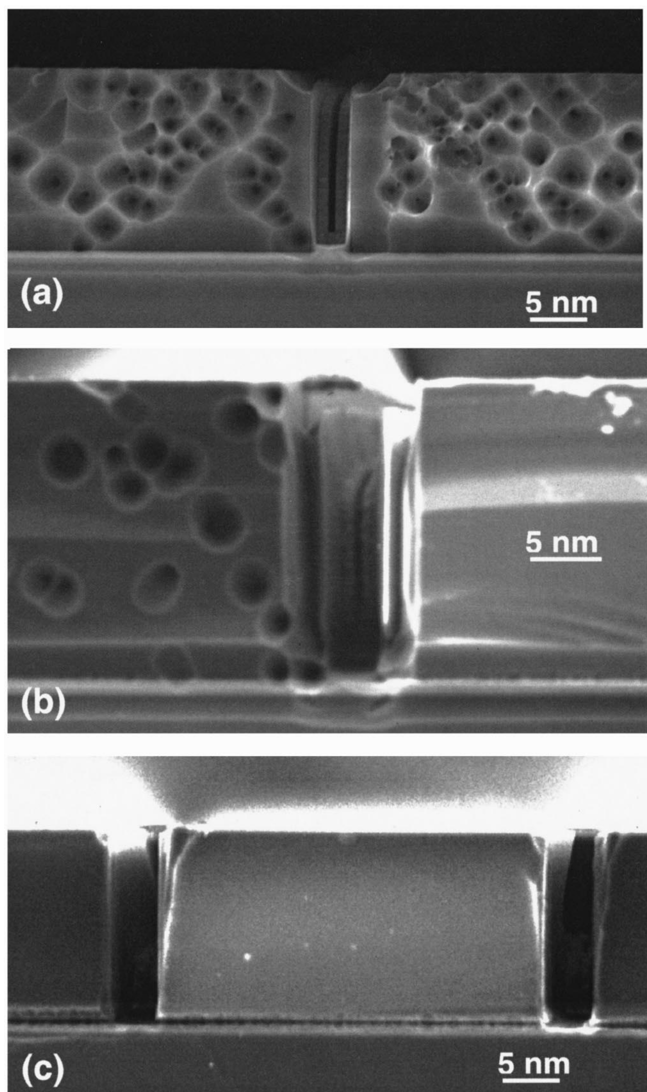

Figure 5. Cross-sectional SEM images of Secco-etched trench-filled SOI, showing slip dislocations: (a) 0.01 Ωcm B-doped (100), (b) 35 Ωcm B-doped (100), and (c) 0.04 Ωcm Sb-doped (111) silicon.

seen in the SOI layer, emanating from both the top and bottom corners of the trenches, as well as at other points along the sidewall, SOI surface and bonding interface. The lightly boron-doped wafer shows a much lower level of slip, with dislocations occurring only at the highly stressed regions near the trench bottom corner. In the case of the antimony-doped wafer [Fig. 5c], the defect etch confirms the absence of slip dislocation generation for this material.

A comparison of the relative ease of slip generation for (100) and (111) crystal orientations can be made in Table I, for the arsenic- and antimony-doped material. For both types of dopant, the (100) orientated silicon appears to have slightly less resistance to the onset of slip than the (111) silicon. However, once slip has occurred, additional slip lines are observed at the surfaces of the (111) wafers, running diagonally across the tubs, as shown in Fig. 4c. This would be a practical concern for fabricating devices, because it would be more difficult to design device components outside the slip areas in this case, compared to samples with (100) orientation.

Figure 6 shows the percentage slip after final densification plotted against the dopant concentration. There is no obvious correlation between these, and indeed the general trends are opposite to those which might be anticipated from the known dependence of yield stress or dislocation velocity on doping, or more precisely on the

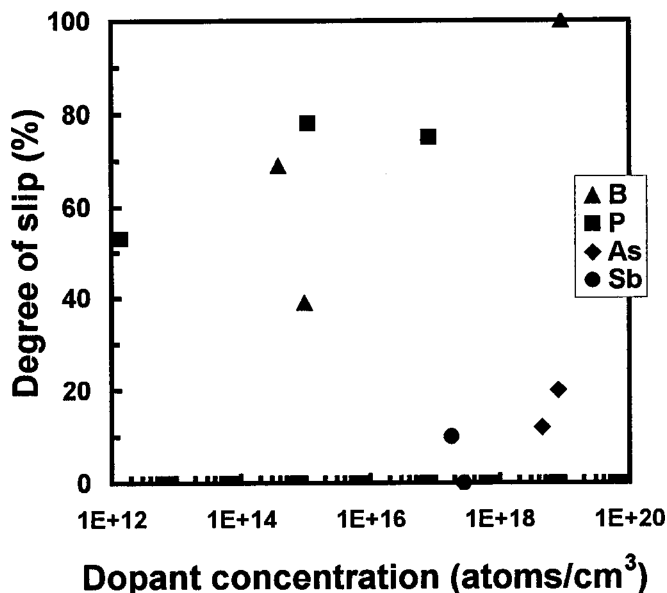

Figure 6. Degree of slip after final densification as a function of doping concentration for trench-filled SOI with various device layer dopants.

position of the Fermi level.[10] Briefly, Hirsch's theory[11] supposes that the activation energy for the formation of kink pairs is lowered if the kinks are charged. Given that there are deep levels associated with these kinks, the concentration of charged kinks will depend on the position of the Fermi level. Thus, in general, yield strength will be greater or less as the concentration of dopant atoms increases in p-type Si (B) and n-type Si (P, As, Sb), respectively. Therefore, if the Fermi level were determined by the doping level one would expect a positive slope in the data in Fig. 6, except for the B-doped samples for which the slope would be negative. This is clearly not the case, because the more heavily doped arsenic and antimony material shows much less slip than the lightly doped phosphorous samples.

However, slip in these experiments is almost certainly occurring at temperatures between 700 and 1050°C, and at these temperatures the Fermi energy is pinned at approximately mid-gap by the large intrinsic carrier concentration. This is true for all samples with concentrations less than $10^{18}/cm^3$. Hence, we do not believe the effect of the doping level upon slip generation to be an electronic effect in the sense of the Hirsch theory. We expect the dislocation mobility to be approximately the same in all samples at the temperature of deposition and densification. We suppose, therefore, that slip generation is controlled by dislocation generation rather than by mobility.

With this in mind, we regard the data in Fig. 6 as falling into three categories

1. The $9 \times 10^{18}/cm^3$ B-doped specimens slip readily after only liner deposition. These were also the only specimens to show a high density of oxygen-related defects after thermal oxidation ($9 \times 10^5/cm^2$, compared to around $2 \times 10^3/cm^2$ for the other groups; see Table I). The generation of these defects is known to be enhanced in heavily B-doped Si, and to nucleate dislocations during precipitation by prismatic punching.[12] Therefore, in these samples a high dislocation density has been created during the bond-anneal processing, which has, in turn, led to a resulting high incidence of slip.

2. The remaining B- and all the P-doped samples fall into a second category, showing some 40-80% slip at the end of the processing, with no clear dependence on dopant concentration. While two moderately doped phosphorous groups with more than two orders of magnitude difference in doping level showed little difference in slip behavior, two B-doped groups with similar dopant concentration nevertheless showed a large disparity in the amount of slip.

The P-doped specimens with a concentration of $1.4 \times 10^{12}/cm^3$ are essentially intrinsic, and we expect all the crystals to be practically dislocation free as-received. We propose that the slip generation is controlled by dislocation generation at the Si-SiO_2 interface. Therefore, the amount of slip generation in this category reflects the ability of the Si-SiO_2 interface in intrinsic materials to nucleate dislocations under stress.

3. The As- and Sb-doped samples fall into the third category whose slip generation is much less, even than the intrinsic Si. Assuming our postulate that slip is generated by dislocation nucleation at the Si-SiO_2 interface, it appears that As and Sb are able to inhibit dislocation nucleation by some mechanism currently not understood. Because it is known that As segregates to the Si-SiO_2 interface during annealing,[13] we can speculate that the size differences between As or Sb and Si might allow interfacial stress to be relieved if these dopants become segregated to the interface at high enough concentrations. If this stress is responsible for dislocation generation, then the dopants would indeed reduce the amount of slip.

A study of slip behavior in silicon would not be complete without considering the possible influence of oxygen in the material, both as interstitial oxygen and in the form of oxide precipitates. As seen in Table I, the levels of oxidation-induced defects generated in the various CZ materials by high-temperature oxidation treatment are, apart from the heavily doped boron samples, low and of the same order. This indicates a negligible influence of oxygen precipitates on the slip dislocation results for this range of materials. In addition, we measured the oxygen content of the silicon material in the SOI layers using SIMS, and these results, adjusted to the new ASTM infrared standard, are also included in Table I. Among the CZ materials, no obvious dependence on oxygen concentration is seen, with the possible exception of the highest-resistivity boron group. This shows a greater susceptibility to slip than the 14 Ωcm boron group, which might be a result of its lower oxygen level. Comparing the FZ material, which has at least an order of magnitude lower oxygen content, there is no obvious effect, in that the degree of slip lies at similar levels to the moderate-to-low doped boron samples. However, there may be subtle differences related to the growth method, such as seen in the tendency for FZ wafers to show higher initial slip generation at the liner densification stage compared to CZ. To ascertain the exact influence of the growth method will require a more detailed comparison of FZ and CZ materials, in which the other parameters are kept essentially the same.

The overall picture we have, therefore, is that large stresses due to mismatch in thermal expansivity arise at the Si-SiO_2 interface which are relieved by slip. Measurements by Baumgart *et al.*[4] have shown tensile stresses as large as 500 MPa in trench isolation structures similar, although smaller, than ours. Except for the heavily B-doped samples, the dislocation density present after bonding is too low to allow general yielding, and the amount of slip is then controlled by the ease of dislocation nucleation at the Si-SiO_2 interface. It is possible that As and Sb could segregate to the interface and inhibit dislocation nucleation.

Effect of buried implants.—We attempted to create a high level of dopant in the SOI layer at the bonding interface by implanting phosphorous-doped material with various dopant species. Table II summarizes the slip results, as well as minority carrier lifetimes and oxidation-induced defect densities for SOI with buried implanted layers of boron, phosphorous, arsenic, and antimony. Note that in this group, the TEOS liner thickness (0.55 μm) is lower than for the samples in Table I, and, hence, less stress is generated at the trench bottom. Three main effects of the buried implant are apparent. The implanted samples show an order of magnitude lower density of oxidation-induced defects than the control wafers, while in the case of the As and Sb implants, there is also a large increase in the measured minority carrier lifetime. These types of effect have been observed previously in implanted SOI, and have been attributed to gettering of metallic impurities and possibly oxygen by the buried implant.[14] In terms of slip dislocation generation, in contrast to the grown-in doping effects described above, no improvement is seen for the As- and Sb-implanted layers. The unimplanted samples remain slip-free throughout the refill and annealing process, while all the implanted groups show varying degrees of slip, depending on the species type. In this case, the dependence on dopant type is different than that seen in Table I for the grown-in dopants, with both the Sb- and B-implanted wafers being worse than P- and As-implanted samples. Clearly, the introduction of a heavily doped implanted layer must therefore weaken the silicon material close to the bonded interface. This might be due to residual crystalline damage caused during the implant which has been insufficiently annealed, or to stress in the silicon from the presence of the dopant atoms. Notably, the two species showing the greatest weakening effect are those whose bonds with silicon show the largest deviation from the Si-Si bond length. The effect does not appear to be related to oxygen precipitates, because all the implanted samples showed similar, low levels of the order of 10^3 defects/cm^2 after thermal oxidation. To gain insight into the origin of this effect, we examined the structure of the bonding interface of an As-implanted sample by TEM. As seen in Fig. 7, a band of crystalline precipitates of about 8 nm size can be seen in the SOI layer, running parallel to the bonding interface, at a distance of about 50 nm above it, which is the region where the implanted atoms are expected to lie. It is conceivable that the mechanical strength of the silicon in the region of these precipitates might be weakened, thus resulting in a lower threshold for slip formation.

Further work will be aimed at characterizing the nature, extent, and conditions of the formation of these precipitates, as well as concentrating on the Si-SiO_2 interface to characterize its atomic structure and chemical composition in doped structures. It is known that the interface is rather abrupt, that the Si is stepped, and that there is possibly a layer of SiO stoichiometry.[15] It is likely that dislocations nucleate as loops at the steps in regions of high stress, and expand into the Si crystal. We cannot say at this stage how this process depends on interface characteristics or composition.

Table II. Dependence of slip generation, oxidation-induced defect density, and minority carrier lifetime on buried implant species in SOI.

	Degree of slip (%)[a]			Defect density[b]	Lifetime[b]
Implant species	Liner dep.	Liner dens.	Final dens.	($10^3/cm^2$)	(μs)
none	0	0	0	40	190
B	0	100	100	2	130
P	0	43	47	2	90
As	0	48	49	2	680
Sb	0	88	100	2	370

[a] Trenched SOI with a 0.55 μm thick oxide liner; the SOI material is 3-5 Ωcm phosphorous-doped (100) CZ, with $<7.0 \times 10^{17}$ atoms/cm^3 oxygen content.
[b] After growth of a 0.5 μm thermal oxide at 1050°C.

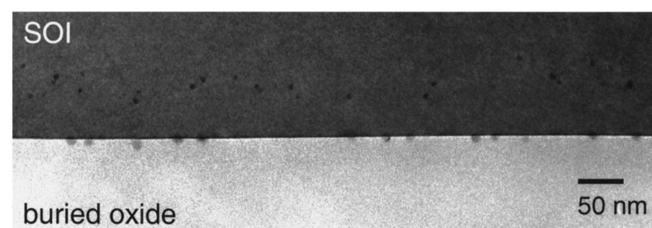

Figure 7. Cross-sectional TEM image of an SOI sample prepared with a $5 \times 10^{15}/cm^2$ dose As buried implant, showing precipitate formation in the SOI layer.

Conclusions

We have observed a strong dependence of the ease of generation of slip dislocations on the type of dopant species in the silicon device material in trenched and refilled fusion-bonded SOI wafers. The material studied fell into three categories

1. Slip generation occurred very easily in heavily B-doped material, being seen at the oxide liner deposition stage. This appears related to a high density of oxygen precipitate-related defects grown during the high-temperature bond anneal.

2. Samples with moderate to low concentrations of B or P showed increasing degrees of slip as the wafers were processed through the refill and thermal annealing cycles. However, there appeared to be little dependence on the dopant concentration.

3. As- and Sb-doped materials were much more resistant to slip than the other materials, with 0.04 Ωcm, (111), CZ Sb samples showing no slip through the complete process. The slip behavior of groups 2 and 3 could not be explained by conventional dislocation mobility theory, but rather the lower occurrence of slip in group 3 appears due to an inhibition of dislocation nucleation in the stressed regions near the bottom corners of the filled trenches. While any influence of growth type (CZ *vs.* FZ) was difficult to ascertain, there did appear to be a small effect of crystal orientation for As and Sb-doped material, where (111) Si material was more resilient to slip than (100). Implanting a layer of dopant into the device at the bonding interface resulted in a significant weakening of the silicon material, with B and Sb implants giving higher slip generation than P and As species. This may be related to the formation of precipitates, seen in the SOI layer near the bonding interface.

Further work on determining the reasons for the observed differences in behavior will focus on examining the structural and chemical characteristics of the Si-SiO_2 trench-sidewall and bonding interfaces. It is anticipated that resolution of this issue can be aided by atomic scale modeling.[16]

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