

HARM Processing Techniques for MEMS and MOEMS Devices using Bonded SOI Substrates and DRIE

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ABSTRACT

Silicon-on-Insulator (SOI) MEMS devices (1) are rapidly gaining popularity in realising numerous solutions for MEMS, especially in the optical and inertia application fields. BCO recently developed a DRIE trench etch, utilising the Bosch process, and refill process for high voltage dielectric isolation integrated circuits on thick SOI substrates (2,3,4). In this paper we present our most recently developed DRIE processes for MEMS and MOEMS devices. These advanced etch techniques are initially described and their integration with silicon bonding demonstrated. This has enabled process flows that are currently being utilised to develop optical router and filter products for fibre optics telecommunications and high precision accelerometers.

SOI MEMS allows thicker structures, common with bulk micromachining, to be integrated with CMOS, as utilised in surface micromachining. The buried sacrificial oxide layer enables 3-D structures to be implemented in single crystal silicon which removes the stress associated with polysilicon. This offers substantial improvements in increased lateral sensitivity for inertia applications and it facilitates the removal of the perforated surface in MOEMS designs by etching through the handle wafer to release the mirrors.

Although the Bosch process was the catalyst that allowed High Aspect Ratio Micromachining (HARM) products to be developed, processes have historically been restricted to bulk micromachining due to the lateral etch characteristics, at the buried oxide interface, for SOI substrates. Several SOI etch processes will be presented that clearly demonstrate the elimination of this notching effect. These applications will include multi feature SOI etching to oxide and through the wafer anisotropic etching.

Keywords: Micromachining, MEMS, MOEMS, MST, DRIE, deep etch, RIE, SOI, DWDM

1. INTRODUCTION

Micromachining is an emerging technology without a global name, Micro-Electro-Mechanical Systems (MEMS) in the US and Microsystems Technology (MST) in Europe. The market, however, is expected to grow to \$38 billion by the year 2002 with an annual increase of approximately 18% (5). Newly developed components will eventually become as commonplace as microelectronics in tomorrows applications. The microelectronics field is exceptionally well-established technology that basically produces electronic circuits on silicon substrates. Micromachining integrates many of these now traditional IC techniques with a complement of new processes to fabricate MEMS devices. Although silicon is not essential to enable these new micromechanical structures to be realised, it dominates over all other material in the micromachining world because it has good mechanical properties and has been substantially analysed by microelectronics professionals for many years. This Semiconductor industry has already developed many of the required processes to manipulate silicon's properties, while also manufacturing cheap high purity monocrystalline silicon starting material.

MEMS are microscopic transducers consisting of electrical and mechanical components, while Micro-Opto-Electro-Mechanical Systems (MOEMS) are generally components that utilise micromirrors to either switch, filter or attenuate the Dense Wavelength Division Multiplexing (DWDM) lightwaves used in fibre optics telecommunications. MEMS fabrication covers three main techniques: bulk micromachining, surface micromachining, and high aspect ratio micromachining (HARM), which includes LIGA and SOI MEMS. Bulk micromachining involves creating the mechanical structure in the initial substrate material, while surface micromachining consists of etching the design into additional films deposited on the wafer surface. Both these techniques have their advantages and drawbacks. Bulk micromachining structures can be manufactured in single crystal material and the structure depth is only limited by the current etch technology. Surface

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micromachined parts are fabricated on a thin deposited polysilicon film on a thermal oxide layer. Although the structure depth is limited by the poly thickness, the oxide layer acts as both an etch stop and a sacrificial layer to facilitate the eventual release of the structure. Unfortunately the thin polysilicon layer restricts the device sensitivity for inertia applications due to limited thickness of the film and the inherent compressive strain. SOI MEMS is an amalgamation of both these techniques that enables very thick structures, hundreds of microns, to be constructed in low stress single crystal silicon, incorporating a sacrificial release layer, which is fully compatible with CMOS processing.

Many of the MEMS technologies incorporate wafer bonding and/or trench etching and can be either integrated into other microelectronic devices or are independent components. This paper will present SOI MEMS technology.

2. SOI FORMATION

Direct wafer bonding, or fusion bonding (6-16), has become an important and increasingly used technique for the manufacturing of sensors and actuators (17,18) and micromirrors to modulate lightwaves (19,20). The technique, Figure 1, offers the possibility of combining different materials and material types, creating buried layers for etch stops or cavities, and hermetically sealed cavities. The buried oxide is first used as an etch stop, allowing features of various geometry to be etched to the same depth, and secondly it is sacrificially removed to release the structure. Fusion bonded SOI offers significant advantages in comparison to polysilicon which is commonly utilised in surface micromachining. The SOI thickness can be actually controlled while minimising stress and defect density, as there are now no grain boundaries. The bonding technique enables easy combination of different material (CZ or FZ), dopant, resistivity and crystallographic orientation.

Initially the handle is thinned to the desired thickness by grinding and polishing. Backside referencing controls the thickness. This is important as when the device and handle are joined; the resulting SOI is thinned to a total thickness using the handle as a reference. This backside referencing and is an essential feature of all grinding technologies.

$$\text{SOI Thickness} = \text{Total Thickness} - (\text{Handle Thickness} + \text{Buried Oxide Thickness})$$

The handle wafer is placed on a rotating chuck beneath the grinding wheel of the grinder, a Shibayama VG-202, Figure 2. The grind wheel is positioned so that the centre of the cutting blade is over the centre of the wafer. The grind wheel then cuts from the centre to the edge of the wafer in a thin slice. The grind wheel is fed vertically down into the wafer allowing it to cut any specified depth with a single grind spindle. This technique causes low sub-surface grind damage and surface roughness while maintaining total thickness variation (TTV) of 0.5 μm . The TTV is defined as the difference between the maximum and minimum thickness of the wafer and this flatness is determined using an ADE UltraGage 9500 measurement tool. The wafer is then polished using a Westech 372, a Chemical Mechanical Polishers (CMP), and this process is essentially designed to remove the sub-surface grind damage and improve the surface roughness. Typically, there remains about 1-2 μm sub-surface damage on a post ground wafer and this is removed during the polish process.

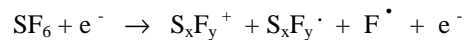
Silicon fusion wafer bonding has become an increasingly important technique in the manufacturing of micromechanical devices. Although this technology for joining smooth surfaces of solid material has been known for several decades, it was re-invented in 1985 by Lasky (6) for use in the electronics industry. The technology relies on the adhesion between extremely smooth and flat silicon surfaces, contacted at room temperature and then permanently joined during a high temperature anneal. The room temperature adhesion is due to the Van der Waals attraction between the species terminating the silicon surface. Generally the surfaces are hydrophilic through a cleaning step and this leaves the surface covered in OH groups. This is done with the bare silicon device wafer and the oxidised handle. The OH groups then form hydrogen bonds when the surfaces are brought into close contact. During annealing the OH groups continue to locate and attract each other and with increasing temperature, water leaves the bonded interface and Si-O-Si bonds are formed. The temperature and duration of this anneal is carefully selected to minimise preferential etching along the bonded surface during HF release. Standard bonding processes, Figure 3, can cause enhanced etching along the bonded interface during HF release. Higher temperatures are preferable as the interface oxide will become viscous and this enables microvoids to become completely sealed at the bonded interface, which substantially decreases preferential etching, Figure 4. The SOI layer is then ground and polished using a similar procedure as for the handle. Finally it should be noted that the Westech polisher, which has a dual platen system for minimal TTV increase, offers a high degree of wafer flatness and thickness control of SOI wafers. The final SOI layers typically have TTV's of +/-0.5 μm although +/-0.3 μm is possible with process optimisation.

3. THE DEEP REACTIVE ION ETCH (DRIE) PROCESS

Although there are many diverse types of plasma sources, the fundamental processes are either purely chemical, purely mechanical or a hybrid of both mechanisms. The chemical process utilises reactive radicals generated in the plasma which undergo a chemical reaction with the silicon surface which creates volatile by-products that are pumped away. During a mechanical etch bombarding ions are accelerated towards the wafer surface and these ions physically remove material by a sputter action. High aspect ratio processes use both mechanisms, in a hybrid solution, while also requiring sidewall passivation to achieve the desired etch rate, selectivity and anisotropy. This enables precise fabrication for dielectric isolation and MEMS applications. Historically, trench isolation was realised by plasma mode etching, using standard capacitively coupled, grounded electrode etchers. These led to the development of Reactive Ion Etching (RIE) in which the RF power was supplied to the wafer. These etchers employed toxic halogen chemistry, principally chlorine and bromine based, to break the Si-Si bonds with energetic ion bombardment followed by the formation of volatile halide compounds. While this technology has proved successful for a number of low aspect ratio, shallow etching applications, such as polysilicon etching, its extension to high aspect ratio, deep etching, such as trenches, is more problematic. Capacitively coupled plasma RIE etching achieves anisotropy by the use of polymerising etch chemistry coupled with ion bombardment. The sputter etch mechanism from the ion bombarding flux will prevent this polymer film from forming at the base of the trench and allowing the silicon to be etched. However, the ions also attack the masking material, lowering selectivity. To maximise the silicon etch rate (0.3-0.5um/min), high pressures (100-500mT) are required, resulting in loss of anisotropy from short ion mean free paths. This is compensated by using greater polymerisation, which can result in micromasking. To prevent micromasking, the platen bias is increased, leading to bowing of the trench profile and reduced selectivity.

Inertia MEMS applications require high aspect ratio (>20:1), deep (up to 100um) trenches. To economically achieve these trenches requires new processes with high etch rate, high selectivity and independent control of etch rate, base pressure, polymerisation and ion bombardment. In order to meet the challenges of the industry, Robert Bosch GmbH originally invented a fluorine-based chemistry process (21), which retains a high etch rate and maintains anisotropy. Instead of simultaneous passivation and etch, as used in RIE etching, etching propagates using the concept of sequentially alternating between these two isolated mechanisms, etch and deposition. Based on this generic approach STS (Surface Technology Systems) have developed its Advanced Silicon Etch (ASE). The development work was carried out on a STS Multiplex inductively coupled plasma system (ICP), Figure 5, and details of the system have been presented elsewhere (22). The etch and passivation gases are SF₆ and C₄F₈ respectively and are switched by a hardware method. The plasma source is generated by a 1kW RF generator and the platen supply is provided by an additional RF generator. This enables independent bias control to the substrate. The wafer is clamped electrostatically and the temperature of the wafer during processing is maintained at <80 °C by helium backcooling. The process pressure is controlled by a butterfly valve that is operable in two modes, fixed and automatic. In fixed mode, the position of the valve is constant and the pressure during processing is determined by the gas flows and RF powers. In automatic mode, the valve position changes in order to maintain a demand pressure.

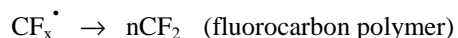
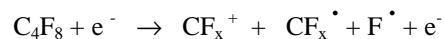
Sulphur Hexafluoride (SF₆) spontaneously etches silicon isotropically by initially dissociating the relatively inert molecule into atomic fluorine radicals:



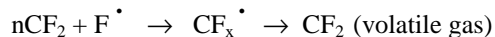
The ion assisted fluorine radicals etches silicon:



The introduction of a short polymer deposition cycle immediately after an etch cycle deposits a layer of passivation (C_xF_y) on the sidewall and the base of the feature, Figure 6, by ionisation and dissociation of octafluorocyclobutane (C₄F₈):



The passivation is easily removed in the subsequent etch step from the base by the ion bombardment and fluorine whilst the sidewall passivation is left intact:



Sequentially alternating the etch and passivation steps, Figure 6, enables the silicon to be etched vertically by restricting the lateral etch characteristic. The process recipe can also be changed in the software and a ramp rate of the various parameters can be set. These combined features enable the ASE DRIE to be manipulated to enable very versatile features to be etched that fully meet the application requirements for many MEMS structures.

This original process technology however, could not be successfully used on SOI wafers because of a severe undercutting of the silicon at the buried oxide-silicon interface, Figures 7 and 8. The undercutting was traced to an accumulation of localised positive charge in the buried oxide, which deflected incident ions towards the trench base sidewall. These deflected ions quickly sputtered away the thin polymer film and exposed the silicon, at the silicon-oxide interface, to attack. In a different approach, BCO worked in conjunction with STS who modified their technology to directly attack the core problem and minimise charging at the oxide interface, within a certain window, by careful selection of process parameters. This enhanced technology (2) minimises localised positive charge build-up in the buried oxide by regularly allowing this inherent charge to dissipate. Therefore, fewer positive ions are repelled into the trench sidewall and the reduced attack of the polymer film prevents undercut at the interface.

4. SOI MEMS

4.1 Discussion

Anisotropic high aspect ratio resonating capacitance structures, accelerometers, with perpendicular beams offer much greater sensitivity, with increased capacitor area, than previous shallower and wet processed designs. HARM inertia MEMS devices are normally fabricated by removing substantial volumes of silicon utilising wet anisotropic technologies like KOH. SOI MEMS, however, is a recent technology that allows thick SOI structures with high aspect ratios that are independent of crystal orientation. When this technology is amalgamated with established sensor designs, it will allow commercialisation of precision inertial sensors, which are a better trade-off between size and cost (17). This technology can easily be integrated into a standard CMOS process as the structural regions are initially isolated by trench and refill before CMOS fabrication. The structures are subsequently etched using DRIE and released in HF by utilising the buried oxide as a sacrificial layer. It is, therefore, very important that an etch process does not cause undercut at the silicon-oxide interface or trench bowing, as this will have an adverse effect on the integrity of the sensors due to variations in the resonant frequency of the capacitance structures.

4.2 Results

These types of structures have been successfully achieved by DRIE of SOI and then releasing the structures by HF removing the buried oxide. Our developed SOI DRIE technology has resulted in a robust one step etch process which has completely eliminated the undercutting problem, without degrading other etch parameters, Figures 9 and 10. These appended micrographs clearly demonstrate that very deep, up to 50 μm , trenches with precise profile control are possible. Optimisation of the trench profile is critical, as it enables voidless dielectric refill for electrical isolating adjacent areas of the structure. This has been engineered by precise process parameter selection and control. We have integrated accurate etch profile tapering, both for the overall trench and at the surface, Figure 11, while minimising sidewall scalloping, Figure 12, with a highly conformal CVD oxide refill to realise voidless fills. The dielectrically refilled trench, Figure 13, is completely filled with CVD oxide without creating voids along the refill seam or inducing dislocations in the SOI layer, although any subsequent high temperature processing may generate slip in the silicon. Utilising a very low deposition rate at low temperature, by significantly increasing the process pressure from the standard TEOS CVD conditions, attained this refill.

The micrographs, Figures 15 and 16, clearly demonstrate that the buried oxide etch stop has enabled both multi features and high aspect ratios to be successfully etched on the same substrate without inducing defects. Such defects include undercut at the Si-SiO₂ interface, profile bowing, residue silicon spikes (or grass) due to excessive passivation, or localised etch alterations due to micro/macroloding or aspect ratio dependence. The free silicon beam, Figure 17, with dimensions of 1mm long by 2 μm wide by 20 μm deep, has been released in HF and this structure confirms the low level of inherent stress within the single crystal silicon SOI layer. DRIE etch processes have also been developed which are capable of successfully fabricating the most challenging design requirements for MEMS applications utilising SOI technology.

Finally some applications require an anisotropic removal of the buried oxide at the base of a feature to enable further DRIE into the handle wafer. This has been accomplished, Figure 14, using Freon chemistry in a standard RIE chamber.

5. SOI MOEMS

5.1 Discussion

The remarkable and relentless increase in Internet usage, with the latest data suggesting that traffic doubles every three months, has caused the major telecommunications companies to invest billions of dollars in optical networking. Multiple signals are simultaneously transmitted on a fibre optic cable using DWDM. In this technique, signals are converted to different wavelengths, or in this case colours, and then the colours are merged and set down the cable as white light, where they are separated at the other end and converted back into multiple signals. The key to this process is the ability to finely discriminate between closely spaced colours and finer discrimination means that more signals can be packed onto a single fibre, and this will subsequently increase the capacity of the system. Furthermore, the transmission technology has evolved dramatically quicker than the switching technology and the current lead-time on the next generation electronic switches is eighteen months while fibre optic data transmission is gaining in popularity and doubles every nine months. Presently DWDM discrimination and switching is done electronically; the light is converted into an electrical signal and then filtered or re-routed using conventional electronic technology. The next generation of optical components will eliminate the requirement to convert the light signals into electronics, before filtering or switching the signal, by utilising micromirrors.

However, it has only been recently possible to fabricate the miniature optical systems to realise this theory. Optical MEMS, or MOEMS, promises to substantially increase existing capacity. There are, therefore, two key MOEMS components that many companies are developing, a filter and router. The filter is to discriminate between the various signals on the fibre and the router will switch between numerous input and output fibres. There are two different switch configurations, $2N$ and N^2 . The N^2 architecture consists of input fibres, output fibres and the set of micromirrors on the same axis with the input and output fibres on orthogonal axes. If the design consisted of 32 input filters with each input fibre having the capability to be switched to any of the 32 output fibres, 1024 micromirrors would be required. The $2N$ architecture, however, differs to the N^2 design as any input fibre has the ability to be routed to any of an array of output fibres, i.e. 1024 micromirrors are only required to enable any single fibre from over a thousand inputs to be switched to any of a similar number of output fibres. It has, also, long been known that if the filtering was done using optical components, before converting it to an electrical signal, finer filtering could be achieved. These components will enable DWDM signals to be modulated without leaving the photonic domain.

5.2 Processing Techniques and Results

The fabrication process utilised to manufacture micromirrors consists of two parts; either a single diaphragm or an array of mirrors and electrodes, or electrostatic actuation, to drive the mirrors. The process flow, Figure 18, involves double-sided DRIE of the handle and SOI layers and then removal of the buried oxide releasing an array of thin membranes, which are connected to the substrate by thin pivotal or support bars. These thin membranes can then be optically coated with a metallic film and act as micromirrors and be tilted electrostatically. To date, large arrays of thin membranes have been manufactured with 100% yield. Initially very deep silicon etch processes were developed that enabled either large or narrow features to be etched through the handle layer, Figures 19 and 20. Initially, the SOI layer is oxidised, patterned by photolithography and RIE before etching the membrane design using the DRIE SOI techniques previously described. The handle layer is then patterned, using an Electronic Visions 420 double-sided aligner tool. Finally holes are etched through the handle to the backside of the SOI layer using RIE and DRIE. The characteristics of the DRIE process were modified to enhance the etch rate by relaxing the control of the scallop size, Figure 21. Precise profile control of these features was not quite as critical as these are normally required as access holes to the backside of the SOI layer. This enables the sacrificial oxide to be stripped from the backside and hence removes of the perforated surface common with the polysilicon surface micromachining approach.

There were many challenges to develop these very different DRIE processes. When the exposed percentage of silicon was very high, approximately 75% locally, causing loading effects which has an adverse effect on the uniformity of the etch. This ultimately causes areas of the silicon to be completely etched to the buried oxide long before other areas are exposed. It is also desirable to minimise the buried oxide thickness as this oxide induces stress in the thin silicon membrane layer due to the difference in thermal expansion between the silicon and buried silicon dioxide layers. Optimising the buried oxide thickness and maximising the selectivity of the DRIE silicon process to oxide counteracted these problems allowing released pre metallised mirrors with radius of curvature greater than 1 metre to be produced. The oxide protected mirrors can then be released, on both sides simultaneously, in hydrofluoric acid. Mirror deformation, or doming, is minimised by careful selection of oxide thickness and process integration, prior to release, allowing the induced stresses caused by the individual oxide layers to counteract each other. Secondly, to achieve through the handle, up to 400µm, DRIE processes with aspect

ratios greater than 10:1 involved multi step processing by ramping the pressure down and platen power up. This minimises the anticipated drop in etch rate, corresponding to increasing depth, without inducing sidewall damage or bowing of the trench.

Furthermore, utilising the diversity of designs that are capable by integrating several etch and bonding steps can enable true three-dimensional structures to be constructed, Figure 22. The previous sections have concentrated on post processing of a standard SOI material but the bonding technique offers several interesting possibilities including pre processing and multi layer bonding (23). This pre bond processing may involve patterned or blanket implants, precavitation or patterning of the buried oxide. Complex structures are manufactured by starting with a standard SOI substrate with a thick buried oxide, then growing a second oxide on the SOI layer, which is RIE patterned before bonding and thinning a third layer. The triple layer structure is created by initially transfusing the lithography pattern into the spacer layer as normal by DRIE until the patterned oxide is reached, between the mirror SOI and spacer SOI layers. At this stage the DRIE only propagates further in the areas that have been pre-patterned by RIE, i.e. the pattern in the oxide is then transferred into the mirror layer and the DRIE eventually stops on the original buried oxide between the handle and mirror layers. Integration of all these techniques will finally makes real three-dimensional structures processed in silicon a reality, by combination of established microelectronics processes with the new techniques presented in this paper.

CONCLUSIONS

It is now possible to integrate fusion bonding and precision thinning with pre and post processing by RIE and state of the art DRIE. Although 2.5-D structures, i.e. 2-D with depth, can be fabricated by standard post processing of SOI material to produce high precision accelerometers and gyroscopes for inertia MEMS applications, true 3-D structures are required to realise the structural requirements for many DWDM components. These types of structures can now be processed by dynamic process flow integration of bonding, thinning and etching techniques, Figure 23. Individual processing techniques have now finally been demonstrated that, when integrated, can produce real 3D micromachining structures that are capable of manufacturing optical components, for the DWDM market, based on micromirrors. This type of sophisticated process integration enables components to be constructed in low stress single wafer material and removes the necessity of perforated mirrors surfaces by through the wafer DRIE processes. It is envisaged in the near future that further bonded and thinned layers will be integrated with pre and post patterned silicon that will ultimately enable full MOEMS structures to be processed completely in a single monolithic silicon substrate. BCO have gained vast experience in the previous twelve months developing these multi structures layers. These new enhanced processing techniques can be incorporated into a full 24hours 7days a week manufacturing operation.

ACKNOWLEDGEMENTS

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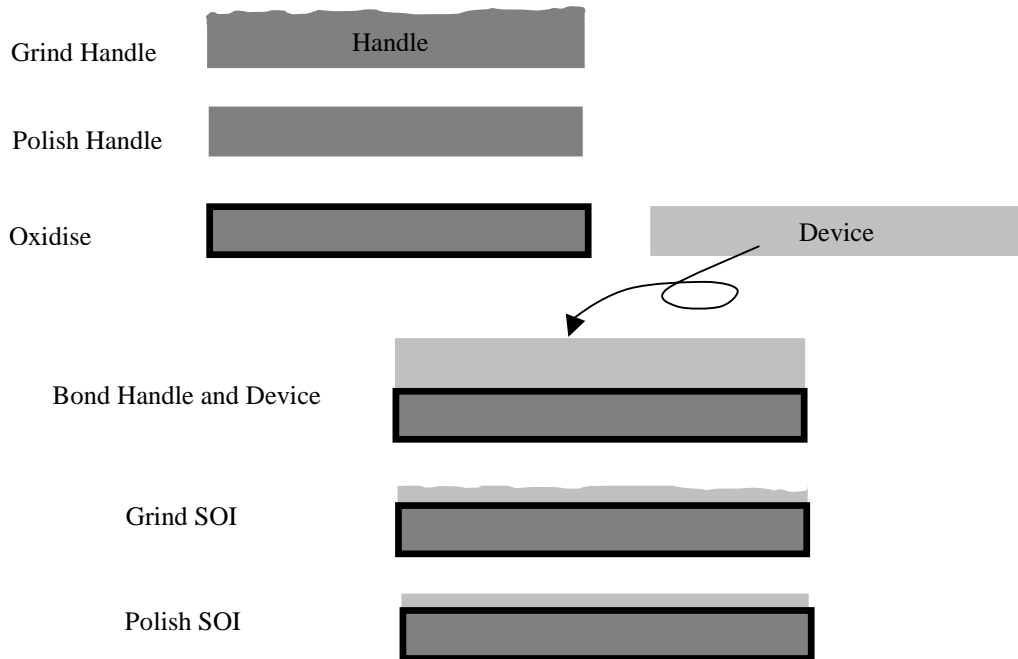


Figure 1: SOI Formation Process Flow

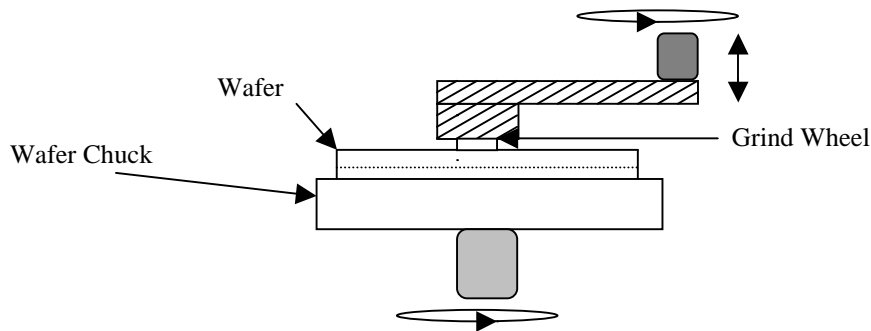


Figure 2: Schematic of Grinder Operation

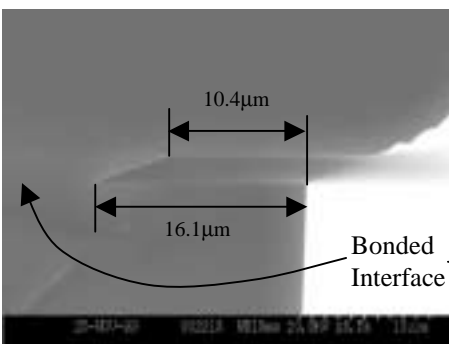


Figure 3: Typical Bonding Process with Greater Than 50% Preferential Etching Along the Bonded Interface.

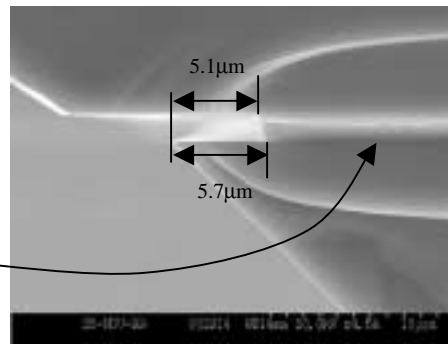


Figure 4: Optimised MEMS Applications Bonding at Higher Temperature. The Preferential Etching has been reduced to Approximately 10%.

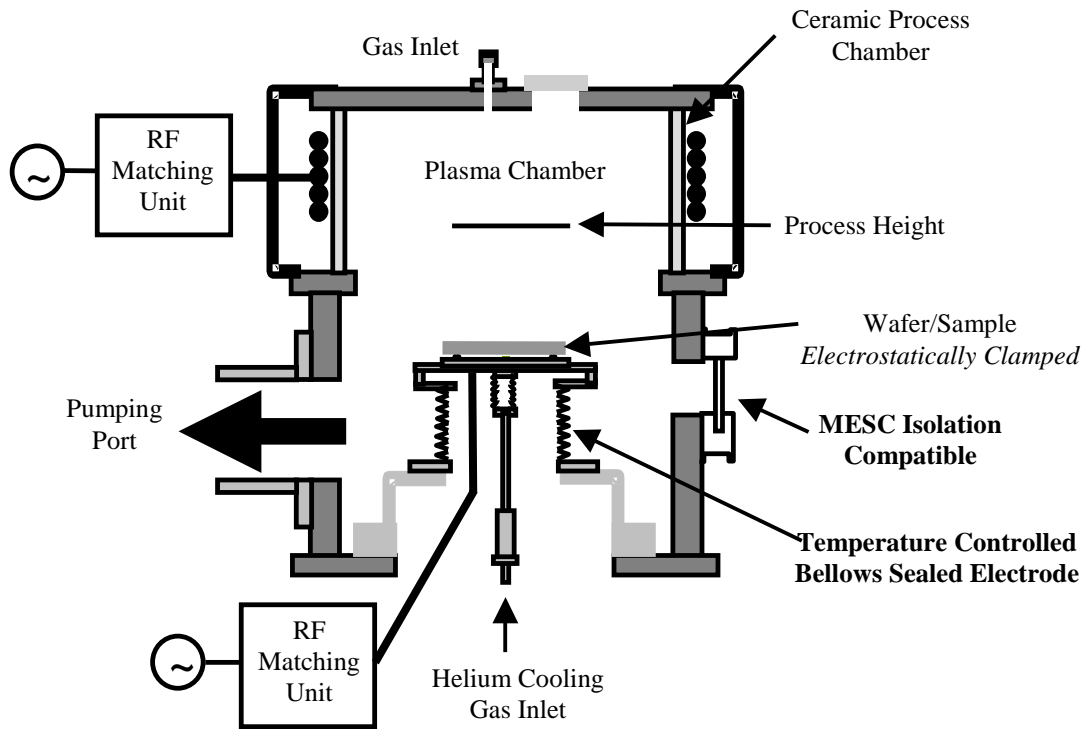


Figure 5: Schematic of Multiplex ICP Process Chamber

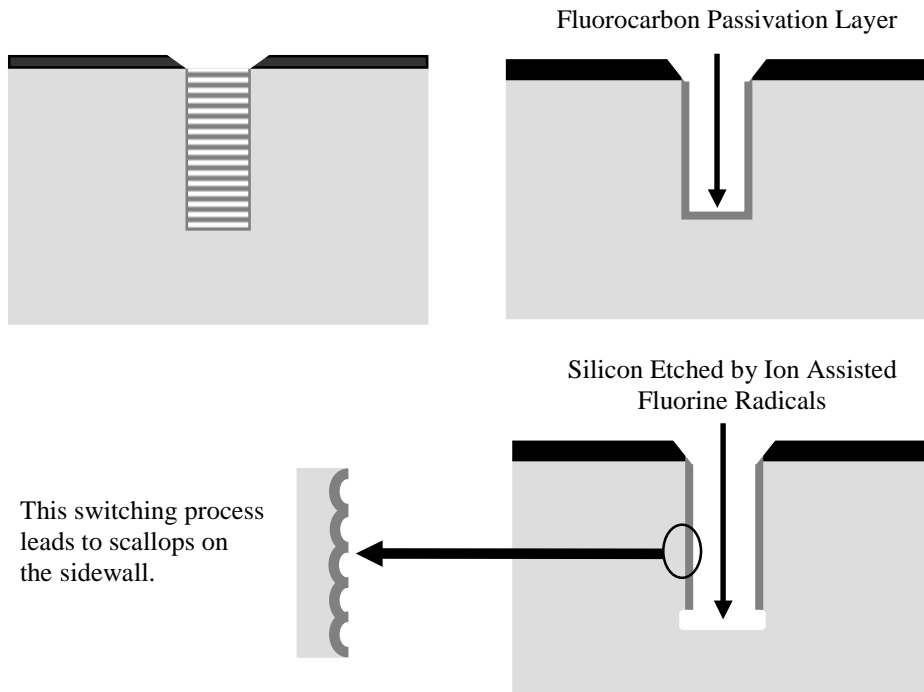


Figure 6: Propagation of the ASE Bosch Etch Process

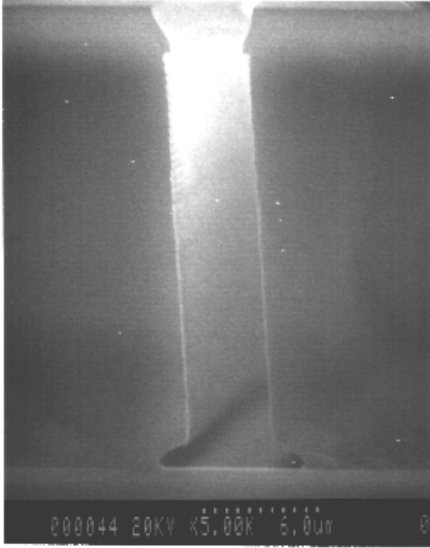


Figure 7: The Original ASE Bosch Process Yielded Severe Undercutting of the Silicon at the Buried Oxide Interface.

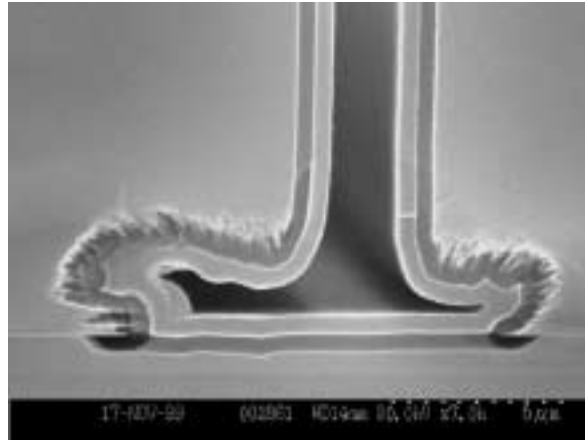


Figure 8: Partially Refilled Trench. Original ASE Process - Undercut Notching Exaggerated by Extensive Over-Etching.

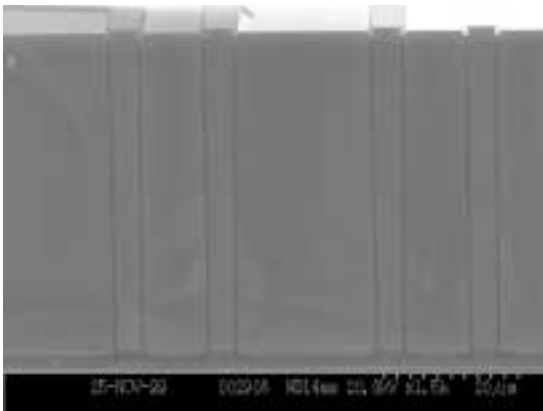


Figure 9: Several 50 μ m Etched and Refilled Trenches with Aspect Ratios Greater than 10. These trenches show no undercut.

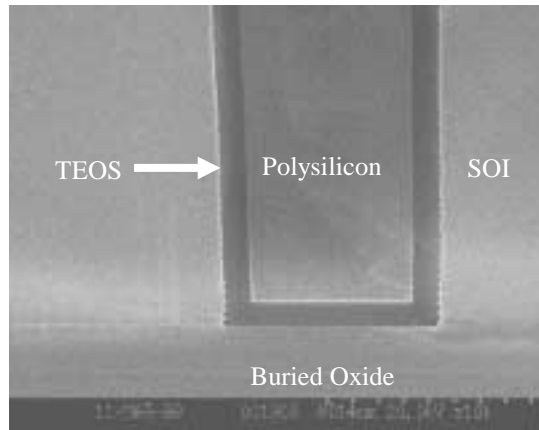


Figure 10: A Blow-up of a Refilled Trench. The Base Clearly Indicates NO Undercut at the Silicon-Buried Oxide Interface.

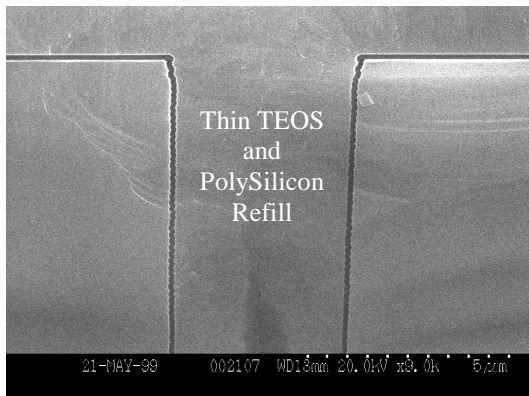


Figure 11: Initial Trench Taper at the SOI Surface Enables Voidless Refills.

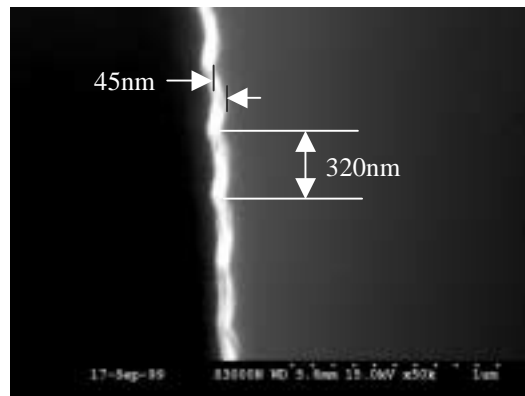


Figure 12: Typical Trench Sidewall Scalloping for Dielectric Isolation. Scalloping is Minimised to Assist Voidless Refills.

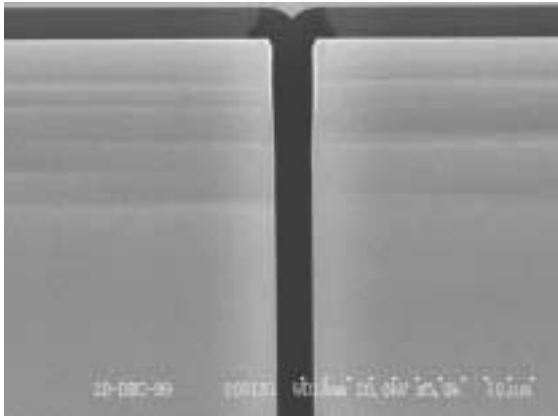


Figure 13: 20µm Trench Refilled Completely with CVD Oxide.

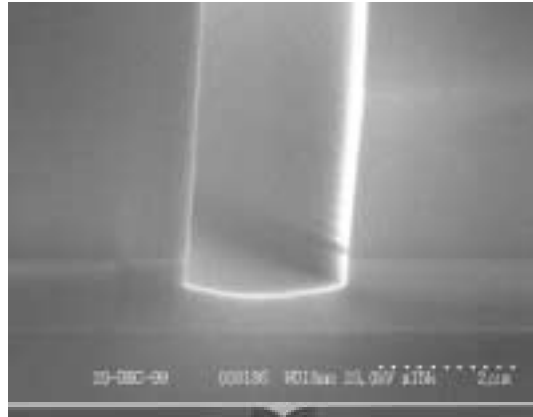


Figure 14: Partially RIE Etched 1µm Etched Buried Oxide

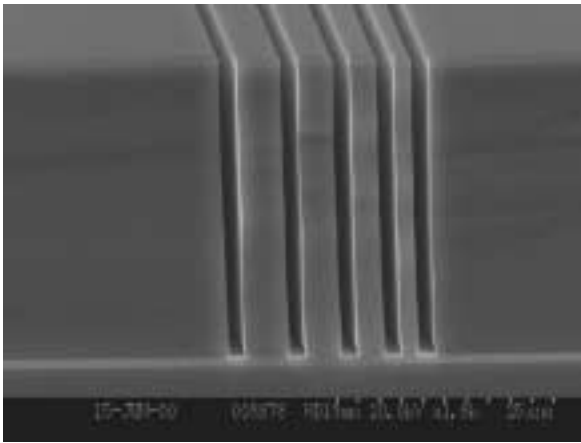


Figure 15: 35µm SOI Etched with an Aspect Ratio of Nearly 20 for Inertia MEMS Applications.

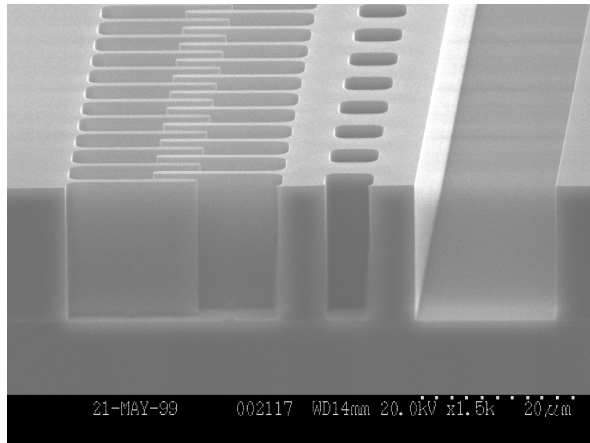


Figure 16: Various Structures Etched in 20µm SOI Indicating NO Defects Generated by the DRIE Process due to Various Geometries.

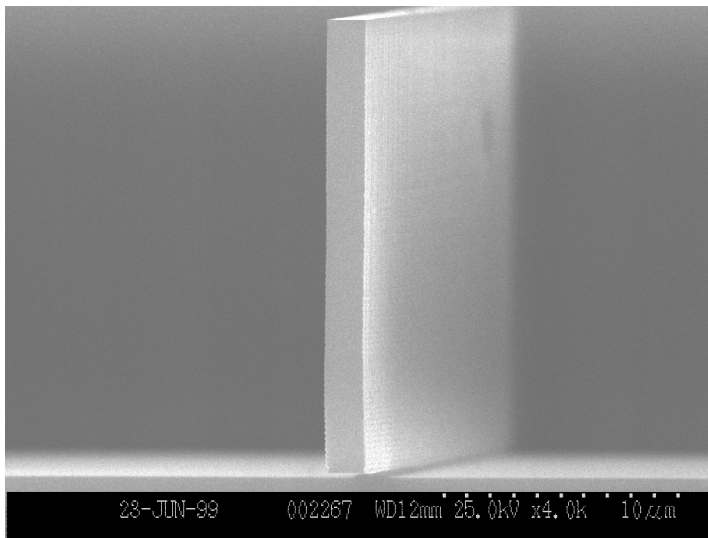


Figure 17: Released Silicon Beam in a 20µm SOI MEMS Structure.

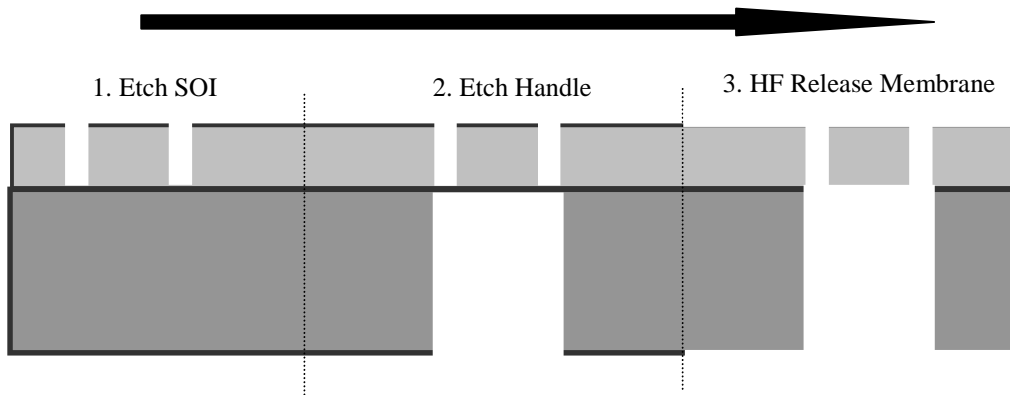


Figure 18: Membranes Created using Double Sided DRIE Processing of SOI



Figure 19: High exposed Area Through the Handle DRIE Process - 350 μ m Deep into a 600 μ m Wafer.

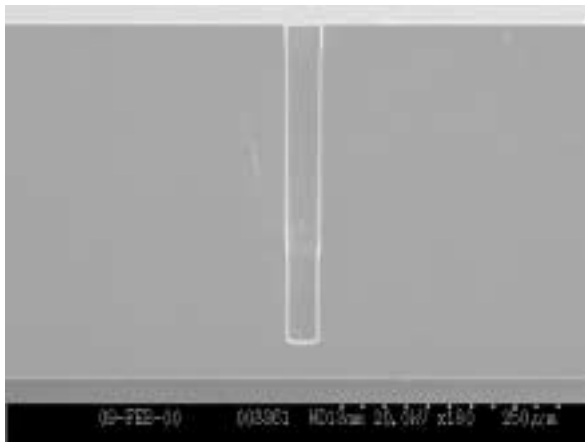


Figure 20: VIA Partially Etched, approximately 360 μ m, Through a 400 μ m Handle.

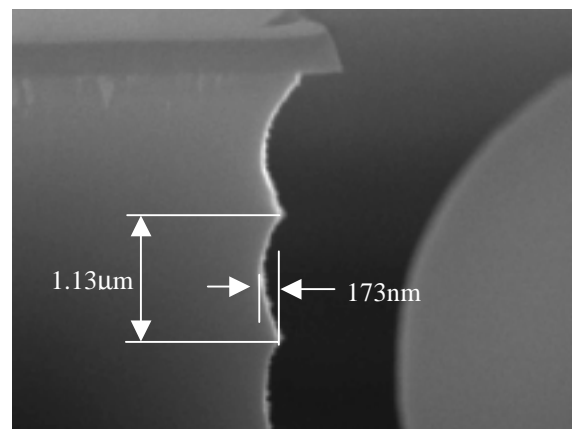


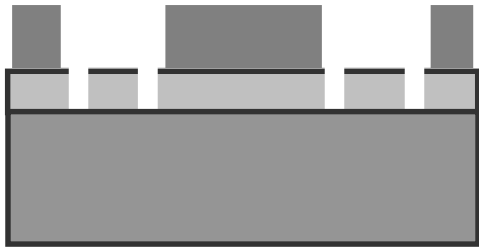
Figure 21: Exaggerated Sidewall Scalloping Created during Aggressive Deep Etching. These MEMS Applications Structures are Etched with an Enhanced Etch Rate and are not Refilled.



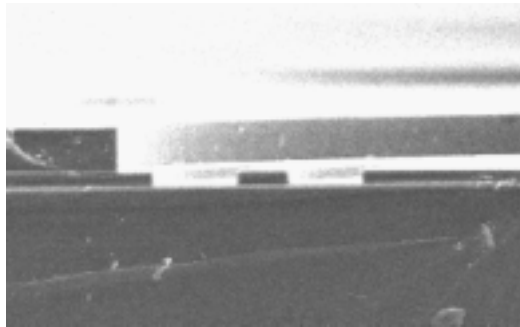
1. Oxidise Standard SOI and RIE Pattern



2. Bond and Precision Thin Third Layer



3. DRIE Both SOI Layers to Enable Structure



4. Micrograph of Completed Structure

Figure 22: Multi Layer Bond and Etch

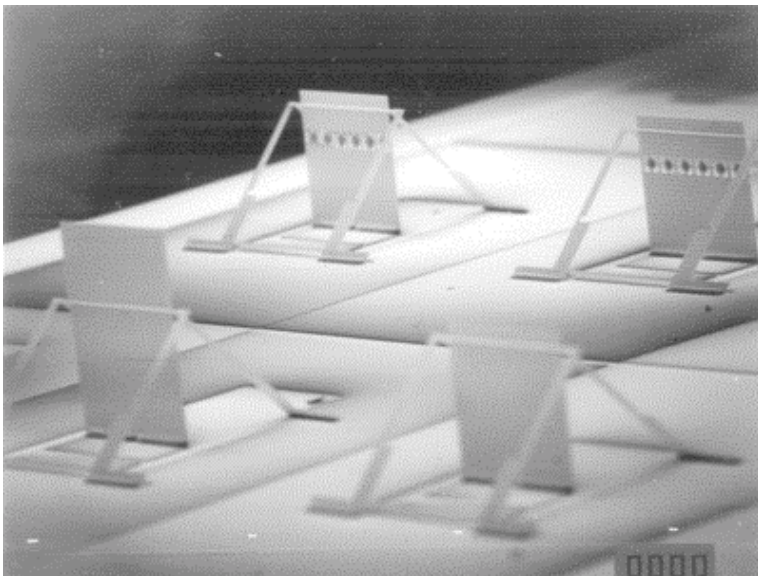


Figure 23: Large Micromirrors created in single crystal SOI using BCO SOI material and DRIE Processing. (Courtesy of Imperial College)