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Integration of high voltage devices on thick SOI substrates for automotive applications

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Abstract

This paper presents a new process for the integration of high voltage devices and low voltage circuitry on thick SOI substrates. Complete dielectric isolation between high voltage and low voltage devices has been realized by deep trench technology. Diodes and transistors with breakdown voltages of 600 and 420 V, respectively, have been demonstrated within these trench structures. © 2001 Elsevier Science Ltd. All rights reserved.

1. Introduction

This paper presents a new process for the integration of high-voltage devices and low-voltage circuitry on thick SOI substrates intended for automotive electronics. SOI technology combined with deep trench isolation allows a complete dielectric isolation between high-voltage and low-voltage devices, enabling the integration of more functions on the same chip. Electronic control units for automotive applications, for example, have to be placed close to or even on top of the engine, where the devices are operated in a harsh environment. Not only the increased temperature requires new solutions for electronic parts, but also vibrations and electromagnetic compatibility are of big concern. High-level integration offers the possibility to reduce cabling and the number of electrical connectors, thus reducing cost and space demand and increasing reliability.

2. Process description

The total galvanic isolation on SOI substrates allows the implementation of lateral and vertical devices. The challenge to realize a vertical device on SOI lies in the

reduction of the on-resistance R_{on}. Therefore we have implanted arsenic into the device layer before bonding, forming a buried n^+-layer (see Fig. 1). Arsenic has a small diffusion constant, thus the doping profile will not smear out as much as a phosphor implant.

The thickness of the buried oxide (2 μm) has been chosen to meet the breakdown voltage (BV) requirement of 400 V and to reduce the capacitive coupling to the substrate. The doping concentration (4×10^{14} cm^{-3}) and thickness (50 μm) of the device layer have been determined to achieve a high BV and a low on-resistance [1].

Electrical isolation in the lateral direction is obtained by etching deep trenches around the high voltage transistors all the way to the buried oxide [2]. The trenches are filled with silicon dioxide and polysilicon. The thickness of the silicon dioxide has been chosen to meet BV requirements yet avoiding to create too much stress. The trench walls are an active part for a vertical device on SOI, because the drain contacts are placed on the topside of the chip. Therefore a high concentration of phosphor has been diffused into the trench sidewalls to decrease R_{on}. The thick SOI material used in this work has been obtained from BCO Technologies.

The implementation of vertical high voltage devices on SOI requires a careful design of the different doping areas. The distance between the source and drain contact has been reduced by including a reduced surface field (RESURF) termination area [3]. We have fabricated terminations with a constant doping profile, with a

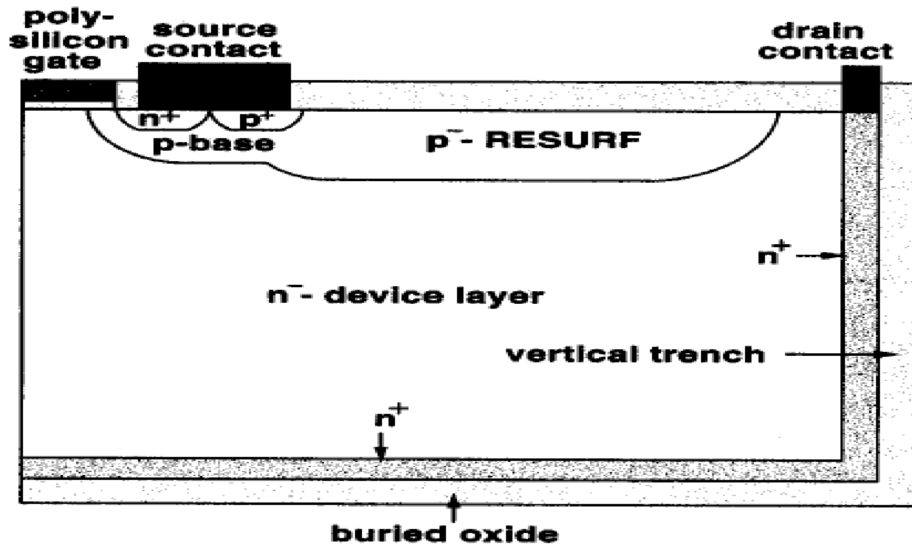

Fig. 1. Schematic drawing (of the right half) of the vertical DMOS transistor on a SOI substrate.

step doping profile and with a variation of the lateral doping profile [4]. The length of the termination with a step doping profile could be reduced by 30% compared to the uniform doping. The optimum termination would be the graded doping profile but due to limitations in the lithography a further reduction of the RESURF area could not be achieved.

The thickness of the SOI layer and the depth of the RESURF termination have been chosen to avoid a punch through of the depletion region in the vertical direction. The dopands in the RESURF area have been annealed for 15 h at 1200°C after implantation and reached a depth of 8 μm. The diffusion of the p-base has been chosen to reach a certain channel length (1 μm) and a certain depth. The electric field will be higher at the corner of the p-base. Therefore a certain depth is necessary to achieve a proper rounding, which will prevent a premature breakdown in this area.

Fig. 2 shows the potential distribution for an applied voltage of 515 V right before breakdown. It can clearly be seen that the RESURF termination leads to a uniform distribution of the potential lines. The simulated *IV*-characteristics are shown in Fig. 3.

All contacts of the structure are at the surface of the wafer. This offers the possibility for simple packaging (flip-chip) and effective cooling of the chip.

3. Results and discussion

In order to implement vertical DMOS transistors on SOI we have fabricated a number of devices. We have

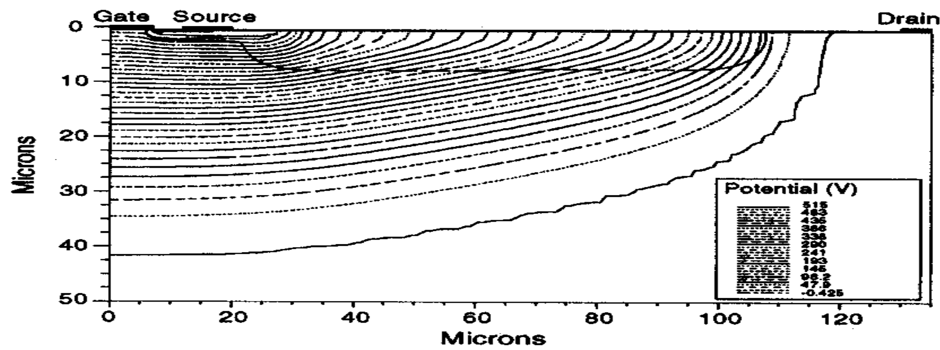

Fig. 2. The RESURF termination results in a uniform distribution of the potential lines.

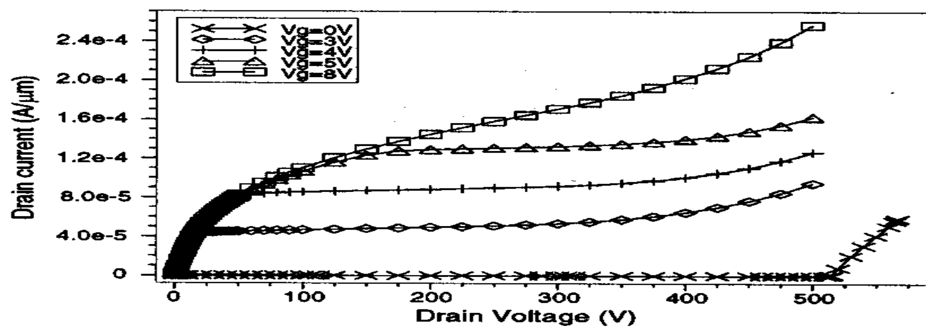

Fig. 3. Simulated *IV*-characteristics of the vertical DMOS transistor on SOI.

chosen a cellular layout to support a given current rating. Furthermore, using a cellular layout with a large number of cells lowers the specific on-resistance, because the area used for the peripheral RESURF termination decreases in proportion to the active area. Fig. 4 shows the top view of a device with 267 cells.

The results of the electrical measurements are shown in Fig. 5. The measured on-resistance is higher compared to the simulations. We believe that this depends on parasitics in the contact areas. The BV of these devices (420 V) is lower than predicted by the simulations. A BV above 600 V could be achieved for diodes consisting of the p^--RESURF implantation and the n^--substrate, shown in Fig. 6. The higher BV of the diodes, compared to the transistors, indicates that the breakdown of the transistor occurs at the corner of the p-base and not at the edge of the RESURF termination.

We started the fabrication process with the etching of the trenches. It turned out that the following high temperature steps (e.g. diffusion of the RESURF termination) create defects in the device layer. Therefore we will

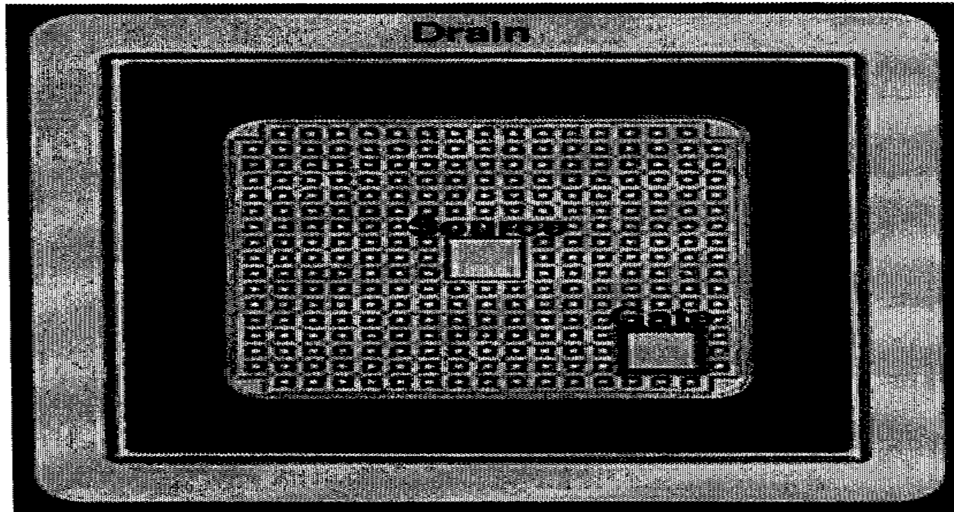

Fig. 4. Top view of a transistor with 267 cells.

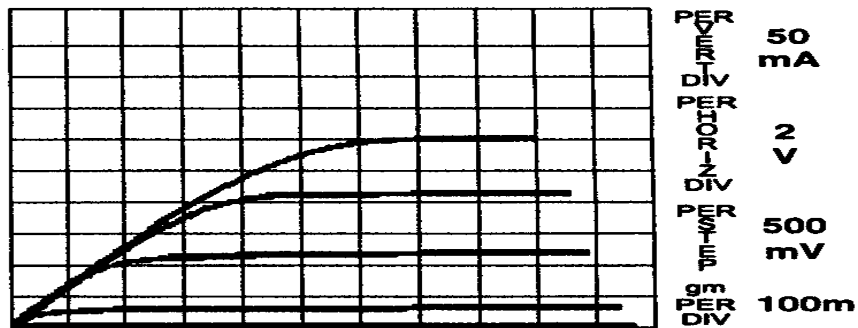

Fig. 5. *IV*-characteristic of a vertical DMOS transistor within a trench structure.

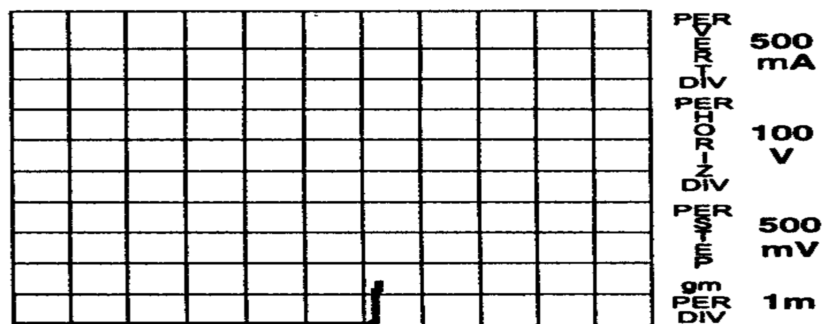

Fig. 6. Breakdown voltage measurement of s p^{-}–n^{-}-diode within a trench structure.

change the process flow in the way that we etch the trenches at the end of the process.

The etching of trenches on SOI substrates in an inductively coupled plasma etcher could not be achieved in a one step process. Due to an accumulation of positive charge in the buried oxide [5] an undercutting of the silicon occurs (see Fig. 7). Fig. 8 shows filled trenches etched by BCO Technologies with a multi-step process.

Integration of high voltage devices and logic circuitry on the same chip requires a CMOS compatible process. Therefore we have included several other devices on the test chip, like nMOS and pMOS transistors, LDMOS transistors, and diodes, to demonstrate the CMOS compatibility. The pMOS devices use the n^--substrate and the nMOS devices the p^--RESURF implants as n-, respectively, p-well. Both types of devices are fully functional.

We have also investigated breakdown behaviour of the trench structures. Devices with one, two and three

Fig. 7. Undercutting of the silicon due to an accumulation of positive charge in the buried oxide.

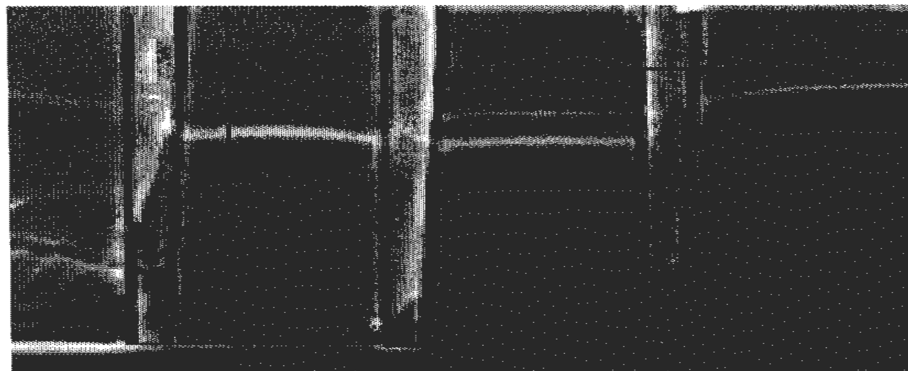

Fig. 8. Trenches etched with a multi-step process and filled with silicon dioxide and polysilicon.

Table 1
BVs of different trench structures

Trench width (μm)	BV of a single trench structure (V)	BV of a double trench structure (V)	BV of a triple trench structure (V)
4	410	540	680
5	440	590	730

trenches have been included in the layout. Table 1 summarizes the BVs. However it is not clear where the breakdown occurs. It could be due to surface defects or bulk defects.

4. Conclusions

A new concept for the integration of high voltage and low voltage devices on thick SOI intended for automotive applications has been presented. Currently we are optimizing the process with respect to on-resistance and defect generation. In addition we have started to investigate the self-heating effects and switching characteristics by means of simulations.

Acknowledgements

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