Bonded Wafers for Use in MEMS Manufacturing

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Abstract

Bonded wafers in general, SOI (Silicon On Insulator) in particular, constitutes an excellent starting material for MEMS manufacturing. This presentation will cover various applications of bonded wafers, as well as material issues and design parameters to consider when manufacturing MEMS using bonded wafers.

Introduction

Direct wafer bonding, or fusion bonding, has become an important and increasingly used technique for the manufacturing of sensors and actuators [see *e.g.* ref 1 and 2]. The technique offers the possibility of combining different materials and material types, creating buried layers for etch stop or contacts, and hermetically sealed cavities.

The technique is very straightforward, but relies on extremely smooth and clean wafer surfaces [3]. The wafers are first brought into contact at room temperature. A van-der-Waals-type adhesion occurs immediately between the surfaces. This weak bond is strengthened during a subsequent anneal [4]. It is important to notice, when dealing with bonded wafers, parameters such as the coefficient of thermal expansion of the various materials. Large mismatch can result in stress, which may affect the device performance. Parameters that should be taken into account when designing a device and/or a process will be discussed below.

Anodic bonding[5], a glass-to-metal sealing technique, is commonly used in MEMS fabrication as well, but mainly for packaging, and will not be discussed in this paper.

As MEMS applications transfer from R&D to production, several advantages can be seen in the use of a pre-processed starting material that already contains some of the features needed in the final process, such as buried layers or cavities. These may easily be included in a bonded substrate. Pre-processed starting material would command a higher price than an unprocessed wafer, but can in many cases result in a lower final product cost.

Bonded SOI Wafers

The most well known type of bonded wafer, is the Silicon-On-Insulator (SOI) [6]. As the name suggests, this refers to a wafer with a thin (a few μm) silicon layer on top of an insulating layer, most often silicon dioxide, on top of a full thickness wafer. See fig 1 for a schematic drawing of the structure. From a commercial point of view, this SOI structure dominates the marketplace although MEMS types of structures are growing rapidly.

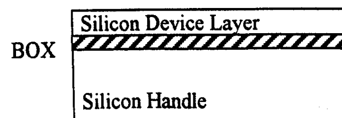

Fig. 1. Schematic drawing of a Silicon-On-Insulator wafer

The substrate, or bottom, wafer is usually referred to as the *handle wafer*, and the thin top silicon layer is called the *device layer*. The wafer used to form the device layer is typically referred to as the device wafer. For MEMS manufacturing purposes, this denomination

may not be completely accurate because the entire, or at least part of, the device may well be made in the handle wafer using the device layer as a kind of lid. Nevertheless this terminology will be used in this paper, for easy reference reasons. The Buried OXide will be referred to as the BOX.

The bonded interface can be located at several different places: at the handle interface, at the device interface, or somewhere in between. This location might be of importance, as we shall see further on. The thickness, resistivity, and orientation of the handle and device wafer, and thickness and composition of the BOX can be varied according to the device requirements almost without restriction.

The thinning of the device can be made in several ways. A common method is to mechanically grind and polish it down to the target thickness. The thickness control in this case is highly dependent on the handle wafer TTV (Total Thickness Variation), since the backside of the handle is used as a reference. To reach TTVs of less than 1 μm, special ultra-flat handles have to be used. In order to make very thin layers, with an accordingly even lower TTV, less than 0.1μm, a further thinning can be made on the SOI wafer by *e.g.* plasma thinning. IPEC Precision has developed a tool specially designed to thin SOI wafers to deep sub-micron tolerances [7]. Another approach to achieving deep sub-micron SOI TTV is to use the SmartCut process [8]. This SmartCut technique was designed to manufacture thin film SOI wafers (typically 0.1μm thick). However, it has been reported that device layers as thick as 1.5 μm are possible.

Advantages

The SOI wafer has by default a built in buried etch-stop layer, the BOX. This can of course be used as an etch stop for either wet or dry etching. An example of this is shown in fig 2, a ring gyro, made by Deep Reactive Ion Etching (DRIE) on a bonded SOI wafer [9]. The BOX was in this case first used as an etch-stop, and later sacrificially etched to release the structure.

Another valuable feature is the well-defined thickness of the silicon and oxide layers. The thickness control depends on the thinning procedure, as pointed out above, and can vary between a couple of hundred Ångström to several μm, depending on the manufacturer.

Single crystalline material offers significant advantages when compared to poly-silicon as in the case of traditional surface micro-machining approaches.

Since the device layer and handle wafer are of bulk quality, the electronic devices manufactured on them use conventional processes and result in performance identical to conventionally processed devices. As a result, in many cases conventionally processed wafers can be used as part of the MEMS structure.

Bulk silicon is also ideal for the mechanical devices because of the low stress and defect density (no grain boundaries). One of the main mechanical advantages that these properties allow is the use of "very large", "high mass" structures. This results in larger signals reducing the demand on the sensing and control electronics thus resulting in lower system cost and complexity while increasing reliability.

The bonding technique enables easy combination of different silicon material types, such as CZ, FZ, different resistivities and dopants, etc. Also, wafers with different crystallographic orientation can be bonded, making possible for instance a (100) device layer on top of a (111) handle. This hetero-orientation can be useful as a KOH etch stop layer for a device in which a BOX is undesirable.

Fig. 2. SEM image of micromechanical gyro, made by Deep RIE on a bonded SOI substrate (© Crown Copyright, DERA, 1997).

Design Considerations

An SOI wafer inevitably contains two different materials - silicon and silicon dioxide - which have different coefficients of thermal expansion. This means that stress will be generated in the interface region. If the stress

becomes high enough it will result in dislocations and stacking faults in the device layer. This may affect the device performance and should thus be taken into consideration when designing the process.

Ways of overcoming problems with a highly stressed device layer may be the use of an oxide grown under special conditions, to achieve a lower coefficient of thermal expansion or perhaps the use of another insulator.

Another issue arising because of a difference in thermal expansion - is the risk of the wafer becoming highly bowed and/or warped. Growing the oxide only on the handle wafer and keeping the oxide on the back of the wafer to balance the BOX may solve this. However, there may be significant problems in cases where the BOX needs to be very thick and/or the design doesn't allow the oxide to be kept on the back. The wafer may be double-side polished or the oxide on the back is attacked in subsequent etch steps. In such cases, it might be worth modifying the process sequence. Perhaps the removal of the backside oxide could be made at a later stage?

Furthermore, having the oxide grown entirely on the handle may be undesirable in that the bonded interface has to be located at the device layer. This may in turn cause other problems. It has been reported that the structural uniformity of this interface is a function of the clean used during the bonding process [10] There have also been reports on break-through of the BOX during wet etching of the top silicon layer, and hence attack of the underlying silicon. It is assumed that these structural imperfections are the reason for the break-through of the oxide by the wet silicon etchant.

To verify this assumption, the following experiment was carried out: Two sets of bonded wafers were made, one where the bonded interface was located towards the handle, and one where it was located towards the device. In both cases they were cleaned with a solution that has been reported to cause structural weakness in the BOX. After grind and polish, the device layer was completely etched away in KOH, and over-etched for 40 minutes. This process resulted in holes in the oxide, which in turn caused etch pits in the handle, on the wafer that had the oxide grown on the device layer, and hence the bonded interface towards the handle. The other SOI wafer did not show any such etch defects. It should be noted that no voids could be seen using SAM (Scanning Acoustic Microscope) inspection after annealing in any of the cases. Interestingly, the structural weaknesses in the BOX do not propagate through the BOX and are somehow "decorated" by the wet etch.

This experiment shows, that in cases were the BOX is used as an etch-stop for a wet silicon etch, it is important to consider both the pre-bond clean and where to place the bonded interface. Obviously, placing the inter-face away from the wet chemical side will result in a more robust manufacturing process.

Bonded Si-Si Wafers

In many cases, it is desirable to have two different silicon materials layered on top of each other without a buried oxide in between. For instance, this allows having a very high resistivity silicon layer on top of a highly doped handle without having to grow epitaxial silicon. This is also known as epitaxial replacement and offers advantages over epitaxy for either thick layers or very high resistivity layers. It also allows the creation of hermetically sealed cavities in the silicon, eliminating the problems that are associated with different thermal expansion properties leading to stress.

What should be considered in the case of silicon to silicon direct bonding is the question of the surface preparation prior to bond. If there must not - for electrical reasons - be any oxide at all in the interface the surfaces have to be etched in HF to remove the native oxide [11,12]. However, such a surface is much more difficult to bond with a high yield than a hydrophilic surface with a thin chemical oxide grown in an oxidising cleaning step.

Added value to the bonded wafer - new possibilities!

The bonding technique offers some interesting possibilities, which show that the bonded SOI wafer can be more than just an SOI wafer. A few of these are discussed below.

Buried implants

For instance, one could include a highly doped layer buried in the device layer. This is made by implantation of the device wafer prior to

bonding [13]. There are several advantages of doing this, as compared to the traditional way of growing epi on top of a doped layer. For instance, it avoids the problem of growing a high quality epi without defects, and the outdiffusion of dopants is not as bad as in the epi-case. A buried implant can also be patterned, giving the possibility of having buried layers of different resistivities and dopant types.

Precavitation

The wafers can also be pre-etched, wet or dry, to form buried cavities. When thinning down the device layer, a thin membrane of the desired thickness will remain above the cavities. It should be noted that while thinning down the silicon, the membrane might start to deflect due to over- or under-pressure in the cavities. These issues can be addressed by a number of techniques such as controlling the composition of the gas in the cavity or by venting the cavity. Membrane stress will also be related to doping and may be used to "tension" a cavity.

Inclusion of other materials

Of course the bonding technique also allows us to combine a wide range of mate-rials. There are publications demonstrating successful bonding of glasses [14], quartz [15], nitride [16], aluminium oxide [17] various metals and silicides [18], *etc*. An example of a third material included in an SOI wafer is the bonded wafer with a buried tungsten silicide at the bottom of the device layer [19]. There are also reports of the creation of buried cobalt and Titanium silicides using wafer bonding [20].

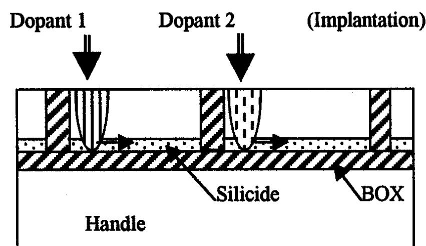

Fig. 5. Illustration of doping of device layer through diffusion in buried silicide.

The silicide has a very low resistivity, and can hence be used as a buried contact. Also, the diffusion rate of dopants in silicide is very high, compared to silicon (10^5), which enables lateral diffusion to distribute the dopant over the entire bottom of the device layer. An annealing step will then cause out-diffusion into the above lying silicon, and hence create a buried high doped region. See fig 5 for an illustration. The buried silicides are also excellent optical reflectors [21] and allow the creation of novel high performance optical devices.

Post-processing

The device layer could be etched and or doped after thinning. An example of such post-bond-processing can be taken from the IC industry. IC manufacturers can buy already trenched wafers for device isolation purposes [22]. Trench technology as developed by the IC industry, was restricted to trench depths of a few microns, insufficient for most MEMS applications. However, recently new trench etching technology has been introduced which allow economical very deep trenches to be etched. Using these techniques it is literally possible to etch entirely through a wafer.

This new trench technology is now commercially available as a service for the fabrication of advanced MEMS structures.

Summary

To summarise, bonded wafers are extre-mely versatile as starting material for a wide range of MEMS as well as IC applications. The use of value added pre-processed wafers makes it even more useful, and allow the fabrication of state of the art MEMS devices without the significant capital requirements that is associated with the fabrication of these structures. However, there are some issues that are inevitably built-in in the bonded substrate, and they have to be taken into consideration when designing the process. Once having dealt with these, though, the possibilities are almost unlimited!

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