

ULTRA-CLEAN Si/Si INTERFACE FORMATION BY SURFACE PREPARATION AND DIRECT BONDING IN ULTRA-HIGH VACUUM

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Silicon surfaces have been cleaned and bonded in Ultra-High Vacuum, at a pressure in the 10^{-10} Torr range. The bonded interfaces show extremely low contamination levels as measured by Secondary Ion Mass Spectroscopy. Nevertheless, a potential barrier could be detected at the interface by spreading resistance and current vs temperature measurements. This suggests that the barrier is caused by inevitable dislocation networks due to wafer misorientation, as well as residual oxygen at the interface.

INTRODUCTION

Room temperature silicon wafer bonding in a clean room environment relies on smooth surfaces, bringing the silicon wafers into close proximity, and a chemical interaction between adsorbed surface atoms and molecules. Direct bonding between the silicon surface atoms is not achieved until a subsequent anneal step. By going to Ultra-High Vacuum (UHV) conditions, wafer bonding can be investigated without the influence of adsorbed surface species. It is well known that impurities present on the wafer surfaces are incorporated into the bonded interfaces (1,2) thereby influencing the interface properties. An open question is what happens if two atomically clean silicon surfaces are brought into contact. In particular, the properties of interfaces formed by bonding of atomically clean surfaces are expected to be an indicator of the intrinsic properties of bonded interfaces.

To date, very little has been done on this subject. Room temperature bonding of silicon at a pressure of 10^{-8} Torr has been reported by Gösele et al (3). In that work the surfaces were prepared by heating of the samples at a pressure of 10^{-8} Torr, and a good bond was achieved as judged from a TEM image. However, to prepare and maintain atomically clean surfaces for reasonable lengths of time, typical UHV pressures of 10^{-10} Torr are required. Recently, we reported the first results on direct bonding in the 10^{-10} Torr range (4). In this work, the direct bonding at a UHV base pressure of 1×10^{-10} Torr, after cleaning at a maximum pressure of 2×10^{-7} Torr, is further investigated. The surfaces were

analyzed prior to bonding by using LEED (Low Energy Electron Diffraction) and AES (Auger Electron Spectroscopy). Chemical analysis of the interfaces formed by UHV-bonding using SIMS (Secondary Ion Mass Spectroscopy) are presented together with electrical data obtained from spreading resistance measurements as well as current vs voltage and current vs temperature measurements.

EXPERIMENTAL

The samples used in the experiments were 1x2 cm pieces of silicon wafers (CZ, (100)-oriented, p-type, 5-30 Ωcm), cleaned in SPM (Sulfuric Peroxide Mixture, of $\text{H}_2\text{SO}_4(97\%):\text{H}_2\text{O}_2(30\%)$, 4:1) for 10 minutes, and rinsed in DI water. The chemical oxide was removed by a 1 minute etch in 10% aqHF, water rinsed and blow-dried in nitrogen. This procedure terminates the surfaces with hydrogen. Immediately after blow-drying, the surfaces were contacted, and a room temperature bond was formed. The samples could thus be transported to the UHV-chamber, not situated in a clean-room environment, without becoming oxidized or contaminated by particles. In the UHV-chamber the samples were mounted on special sample holders that include silicon strips used to heat the samples, to avoid direct current through the samples (4). The sample mounting is schematically shown in figure 1. After reaching the base pressure (1×10^{-10} Torr), the samples were debonded.

In order to prepare a clean and reconstructed silicon surface the following procedure was performed: After debonding the samples were outgassed at 600°C for several hours. After cooling, the surfaces were cleaned by "flashing" to 850°C during short periods of time, to a total time of about 10 minutes. The samples were then allowed to cool for some minutes before the surfaces were brought together, using a micrometer screw feed-through to apply a slight pressure. While pressing the surfaces together a second heat treatment at approximately 450°C was performed.

THE UHV-PREPARED SILICON SURFACE

During and after surface preparation, characterization of the surface condition was performed, using LEED and AES, to make sure that the surfaces were clean at the moment of bonding.

Immediately after debonding it was concluded that the silicon surfaces had not oxidized, since a 1x1 LEED pattern from an unreconstructed H-terminated surface could be observed. The samples were then outgassed at about 600°C for several hours, while keeping the pressure in the chamber below 2×10^{-9} Torr. This should remove the surface hydrogen (5). However, after this procedure, no diffraction pattern could be obtained with LEED, indicating a contaminated and/or disordered surface. AES showed increased amounts of oxygen as well as carbon on the surface.

After a short additional heating for only 2 minutes at 850°C, a diffraction pattern was again obtained, showing a (2x1) reconstruction of the clean silicon surface. The diffraction pattern is shown in figure 2. This observation indicates that the degradation that takes place during heating to 600°C, whether it be a contamination layer or a disordering of the surface

structure, can be removed at a higher temperature. The 850°C is chosen to be above the silicon dioxide sublimation temperature (6).

CHARACTERIZATION OF THE BONDED INTERFACE

The bonded interfaces achieved high mechanical strength, qualitatively judged from the fact that they could withstand a polishing at a beveled angle, as described below. Bonding was not achieved if no pressure or heating was applied. The reasons for this are still not clear, presumably it reflects the need for substantial atomic diffusion to obtain silicon/silicon bonding across the entire interface. The formed interfaces were characterized electrically by spreading resistance, current vs voltage, and current vs temperature measurements, and chemically by SIMS analysis.

Spreading Resistance Measurements

The UHV-bonded interfaces were electrically characterized using spreading resistance measurements. A reference sample was made in the clean-room by HF-etching, bonding and annealing in a conventional furnace (1000° C, 30 min. in N₂). The samples were polished to a beveled angle of 11.54° or 5.45° as a preparation for the spreading resistance measurements. As shown in figure 3, a small resistance peak is observed at the location of the bonded p-type/p-type interface in both samples. No clear differences could be found between UHV and clean-room samples. This means that the surface potentials and the majority carrier concentrations at the bonded interfaces are approximately equal in the two samples.

A more detailed analysis of the data shows that in both cases the increase in spreading resistance corresponds to a barrier caused by an interfacial sheet charge of about 10¹¹ positive elementary charges per cm². This corresponds to an energy barrier of the order of 0.1 eV, which should have a noticeable influence on the carrier transport through the sample at room temperature.

Current vs Voltage and Current vs Temperature Measurements

To verify the results in the spreading resistance analysis, the bonded Si/Si p-type/p-type junctions were characterized using conventional current vs voltage and current vs temperature measurements. The current vs voltage curves of the UHV bonded samples showed the presence of an interfacial barrier influencing the current. Figure 4 shows an activation plot of the current across the bonded interface obtained from current vs temperature measurements at different applied voltages. It is obvious from this figure that the current is thermally activated at lower temperatures. The activation energy is found to be voltage dependent, corresponding to a potential barrier that decreases with the applied voltage. This is what one should expect for a bonded Si/Si interface where the potential barrier is caused by a sheet charge due to interface states, being filled to the position of the Fermi level at the interface (7). From figure 4, an activation energy of 0.11 eV is deduced for the curve corresponding to an applied voltage of 0.1 V. This activation energy is in

agreement with the results of the spreading resistance analysis. At temperatures between approximately 170 and 270 K the current becomes approximately temperature independent, but again shows indications of becoming thermally activated at the highest investigated temperatures. The current vs voltage characteristic also change from emission type at the lowest and the highest temperatures, to a approximately ohmic character at the intermediate temperatures. However, at these temperatures the current across the structure is too small to be explained by the bulk resistivity of the silicon.

SIMS Analysis of the UHV Bonded Interfaces

SIMS (Secondary Ion Mass Spectroscopy) analysis was made to investigate the presence of impurities at the bonded interfaces and to find out the origin of the observed interfacial barrier. The following elements were analyzed for all samples: H, C, O, F, S, Cl (Cs^+ primary ions) and Na, Al, K, Ca, Cr, Fe, Mn, Ni, Cu, Ta (O^- primary ions). The samples were polished in the same way as for the spreading resistance measurements, thereby exposing the bonded interface.

Table I summarizes the SIMS-results for one clean room bonded and several UHV-bonded samples. The value Δ_{signal} given after each element is defined as the approximate ratio of the signals [counts/s] from the peak at the bonded interface and from the bulk part of the sample. Figure 5 shows the peaks from the detected non-metallic and metallic contaminants, respectively, in the UHV-sample "UHV(v)" and in the clean room sample "RR" of Table I.

By doing the SIMS analysis in a spot located slightly above the bonded interface on the beveled sample, bulk silicon is analyzed before passing the bonded interface. Since the sample has a bevel, the cross section of the interface will pass over the analyzed area during sputtering. This is the reason for the broad appearance of the peaks in figure 5. An attempt was made to determine the absolute values of some important impurities by use of known reference samples. This relatively rough estimate gave the result that the concentrations, assuming that they are present in a volume element around the interface, are at least of the magnitudes shown in Table II. The spread in impurity concentrations between different UHV-bonded samples were found to be less than an order of magnitude.

Clearly, the UHV-bonded interfaces are less contaminated than the clean-room ones, although a large spread in results is observed. The samples "UHV(iv)" and "UHV(v)" in Table I were prepared and room temperature bonded in the clean room at the same occasion. The samples show considerable larger levels of, Ca, Na, and K as compared to the other UHV-bonded samples, pointing to possible influences of differences in the wet cleaning procedures on the contamination levels also after cleaning in UHV. The SIMS-results taken together are clear evidence of the effectiveness of the UHV cleaning procedure.

DISCUSSION

The most striking result is that although there is a clear difference (about an order of magnitude) between the interface impurity concentrations in samples bonded in UHV, as compared to samples bonded in the clean-room, the spreading resistance data are very similar. That is, the electrical behavior as indicated by the spreading resistance measurement is about the same, regardless of the impurities at this level. The results show that O and S are present at the bonded interfaces, although the differences are large between the clean-room bonded and the UHV bonded samples. Those impurities may act as donors in silicon, which would give rise to a barrier of the observed type. However, the spreading resistance data for the two cases are very similar. A possible explanation is the different anneal temperatures. A barrier of the observed type would occur if impurities acting as donors, *e.g.* O or S, were present. Since activation and deactivation of different donors occur at different temperatures, it is possible that some of the impurities are electrically active only after the 450°C anneal but not after the 1000°C anneal. It is reported that in CZ material, O could getter and precipitate at the bonded interface during heating (8). A parallel can be made with so called Thermal Donors, observed to appear in SIMOX materials at 450°C, and deactivate above about 650°C (9). Another possible explanation to the similarities in the electrical behaviour is that the potential barrier at the interface is due not to contamination but rather to "intrinsic" factors, such as inevitable misorientation between the wafers and miscut of the individual wafer surfaces, causing dislocation networks in the interface region.

Apparently, the current across the sample is restricted by a potential barrier (10). This potential barrier is relatively low and does not affect the current across the bonded interface at room temperature. Potential barriers at bonded Si/Si interfaces range in amplitude from almost zero to about 0.5 V depending on the cleaning procedure used before wafer bonding (7,10). The barrier found from the spreading resistance measurements agrees with the activation energy obtained from the current vs temperature measurements (figure 4). The current vs temperature curve shows a peculiar behavior at temperatures between 170 and 270 K. Also the current vs voltage characteristics differ at these temperatures as compared to the characteristics at lower and higher temperatures. The reason for this is not understood. One may speculate that different parts of the junction are active at different temperatures.

Another interesting result is that the surfaces are seen to degrade upon heating to 600°C in UHV. This indicates that the surface is disordered (not able to reconstruct) and/or it gets contaminated with some species during the outgassing, that destroys the diffraction pattern. The latter theory is supported by the observation of increased amounts of oxygen as well as carbon on the surface (AES). Sticking of carbon monoxide to the surface could thus be a possible explanation, although the increase in both carbon and oxygen monitored by AES are small. The lack of any visible LEED spots after the 600° C anneal implies that the contaminated or disordered layer at the surface is more than one atomic layer thick. One possible explanation is diffusion of oxygen and other elements from the ends of the 2x1 cm² samples, which are not protected after cleanroom bonding, into the 1x1 cm² central region of the samples where a clear (1x1) LEED pattern is seen prior to annealing. A clean but not ordered (reconstructed) surface could be another possible explanation. Heating to 850° C gives a LEED pattern again, due to removal of carbon and oxygen and/or ordering of the surface structure. Hence, to obtain true Si-Si bonding between the two crystals, the surfaces should be cleaned at about 850°C, at very low pressure. Wafer bonding in UHV does allow studies of direct bonding between surfaces cleaner and more atomically

ordered than is possible by any other method invented so far. An interesting perspective of this work is to attempt to preserve surface reconstructions such as the (7x7) reconstruction of Si(111) at such bonded interfaces, to study their effect on the electrical characteristics of the interface.

CONCLUSIONS

We have shown results on silicon structures formed by wafer bonding in Ultra-High Vacuum, at a pressure in the 10^{-10} Torr range. To obtain clean silicon surfaces before UHV-bonding the surfaces should be cleaned at about 850°C in a pressure below 10^9 Torr. As measured by SIMS, the UHV-bonded interfaces contain more than an order of magnitude less impurities compared to interfaces prepared in the clean room. Nevertheless, a potential barrier could be detected at the interface by spreading resistance and current vs temperature measurements. The energy barrier from both of these analysis is in the 0.1 eV range. It is suggested that the barrier is caused by inevitable dislocation networks due to wafer misorientation, as well as residual oxygen at the interface.

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Table I. SIMS data for differently prepared samples, bonded in UHV and in the clean-room. The values Δ_{signal} given after each element is defined as the ratio of the signals [counts/s] from the peak at the bonded interface and from the bulk part of the sample.

Bonded in [name]	Clean room chemistry	Result SIMS-analysis (Δ_{signal})
UHV [UHV(i)]	SPM + 10% aqHF	K(30), Ca(4)
UHV [UHV(ii)]	SPM	H(10), C(3), O(10), F(10), S(100) Na(8), K(5), Ca(4)
Clean room [RR]	SPM + 10% aqHF	H(40), C(130), O(50), F(10), S(80), Cl(10) Na(1000), K(2000), Ca(1500), Cr(20), (Fe?)
UHV [UHV(iii)]	SPM + 10% aqHF	H(5), C(2), O(10), Cl(10)
UHV [UHV(iv)]	SPM + 10% aqHF	H(3), C(4), O(3), F(2), S(10) Na(200), K(500), Ca(200), Cr(20), Mn(10)
UHV [UHV(v)]	SPM + 10% aqHF	H(6), C(18), O(4), F(5) Na(100), K(150), Ca(10)

Table II. Estimated concentrations of impurities at UHV-bonded Si/Si interfaces.

Element	Concentration (cm ⁻³)	Element	Concentration (cm ⁻³)
Hydrogen	1x10 ²⁰	Sodium	4x10 ¹⁷
Carbon	4x10 ¹⁹	Potassium	2x10 ¹⁷
Fluorine	2x10 ¹⁷	Calcium	2x10 ¹⁷
Oxygen	2x10 ²⁰	Chromium	2x10 ¹⁶
Sulfur	5x10 ¹⁷		

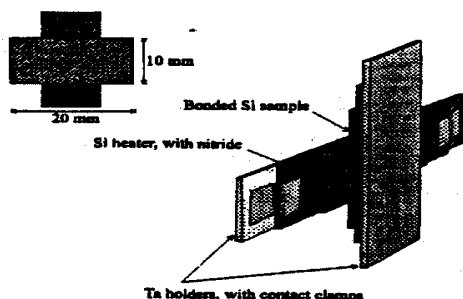


Figure 1. The experimental set-up, showing a perspective view of the bonded silicon sample mounted on the holders with silicon nitride covered heater elements.

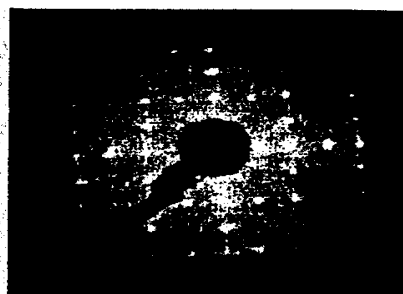


Figure 2. LEED pattern showing a (2x1) reconstructed silicon surface after heating to 850° C in UHV.

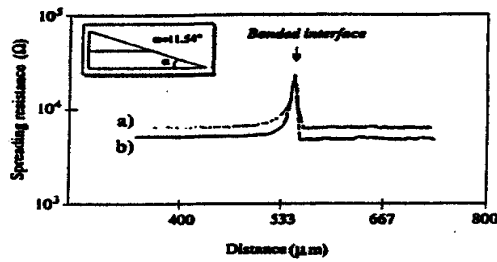


Figure 3. The measured spreading resistances for samples a) cleaned, bonded, and annealed in UHV, and b) bonded and furnace-annealed in the clean-room.

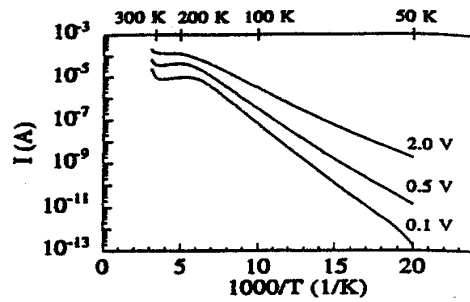


Figure 4. Activation plot at different applied voltages for a Si/Si p-type/p-type junction formed by wafer bonding in UHV.

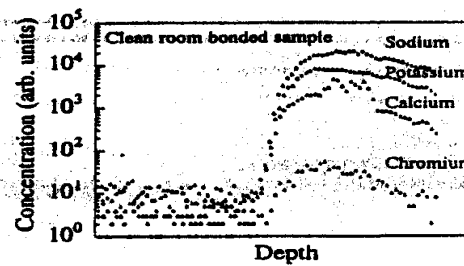
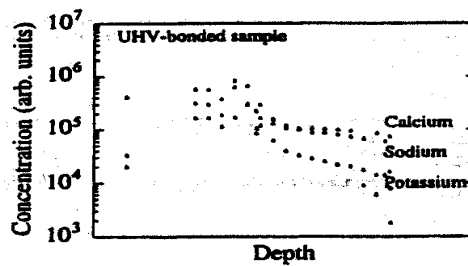
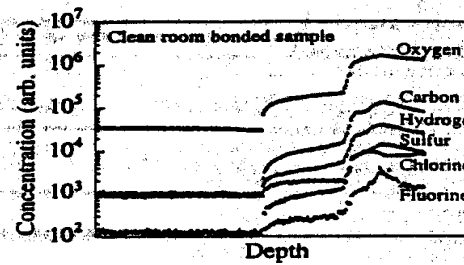
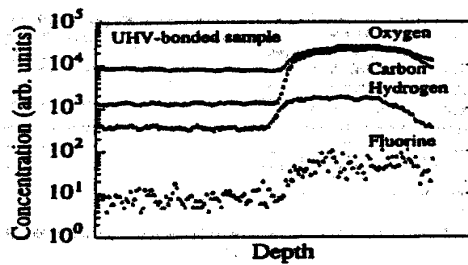


Figure 5. Non-metallic and metallic contaminants, respectively, as obtained from SIMS in the UHV-sample "UHV(v)" and in the clean room sample "RR" of Table I.