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High Speed Bipolar on Bonded Buried Silicide SOI (S^2OI).

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Abstract

High speed bipolar transistors have been successfully fabricated on bonded buried silicide SOI (S^2OI) wafers using a single polysilicon process. The use of buried tungsten silicide resulted in an order of magnitude reduction in buried layer resistance over normal implanted silicon. The material also allows an epitaxy-less bipolar process to be used because the epitaxy is replaced by a bonded active film.

Electrical results exhibit excellent device linearity over many orders of collector current, showing that the active film is uncontaminated by the buried WSi film.

Fully integrated processing with two layers of metal has allowed ring oscillators to be evaluated and demonstrate circuit functionality.

1. Bonded buried silicide

The buried silicide SOI (S^2OI) structure was formed with an active silicon device layer on top of 0.2μm CVD tungsten silicide ($WSi_{2.6}$) as shown in figure 1. The structure incorporated an interfacial layer and a 0.45μm oxide on a silicon handle substrate [1].

To prevent the formation of a Schottky barrier between the tungsten silicide and the

lightly doped n-type active film, an arsenic implant was used prior to bonding [2].

Secondary Ion Mass Spectroscopy (SIMS) was used to show that the active silicon layer was free of any metallic contamination [3]. SIMS also demonstrated that the buried silicide layer was stable at temperatures of over 1100°C with no out-diffusion of the tungsten into the silicon above it.

Mechanical grind and polish was used to achieve active silicon film thicknesses of 1.5μm +/-0.5μm on the buried silicide and oxide as shown schematically in figure 1.

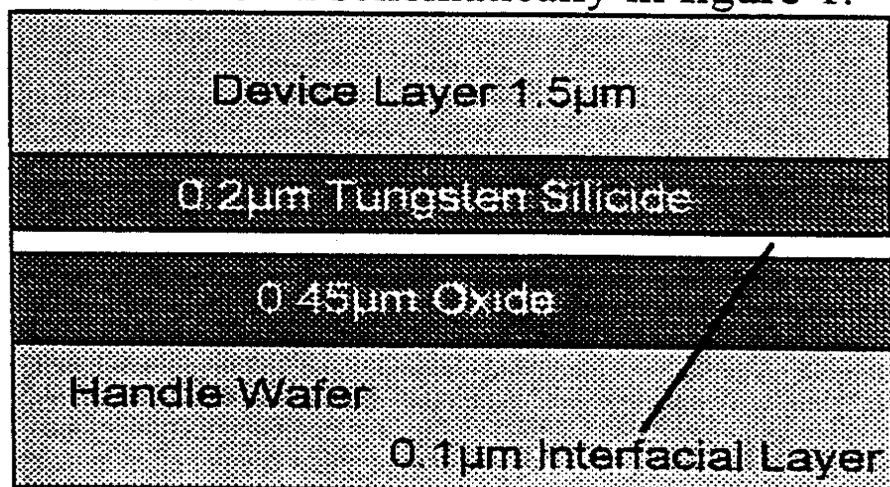

Figure 1. Bonded Silicide Structure

Thicker active films have already been used for smart power devices [4] but we wanted to look at the compatibility with a higher speed bipolar process and a thinner active silicon layer.

2. Bipolar device formation

In order to demonstrate the use of buried silicide a relatively simple device structure was used (figure 2). This was based on a single polysilicon bipolar process [5] with some modifications.

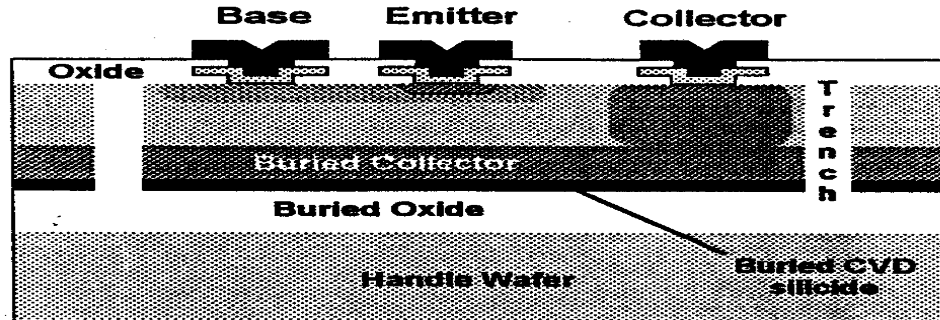

Figure 2 Schematic cross-section of buried silicide SOI NPN device.

The bonded buried silicide SOI wafer was trench etched down through the silicide to the buried oxide. CVD TEOS oxide was used as the trench fill and was etched back level with the surface of the wafer. The base was then implanted into the wafers before depositing CVD oxide and etching contacts. LPCVD deposited polysilicon was then implanted and used to create an emitter. It also served to connect to the base and collector regions of the transistors. The wafers were given Rapid Thermal Anneal (RTA) and metallised (see figure 3).

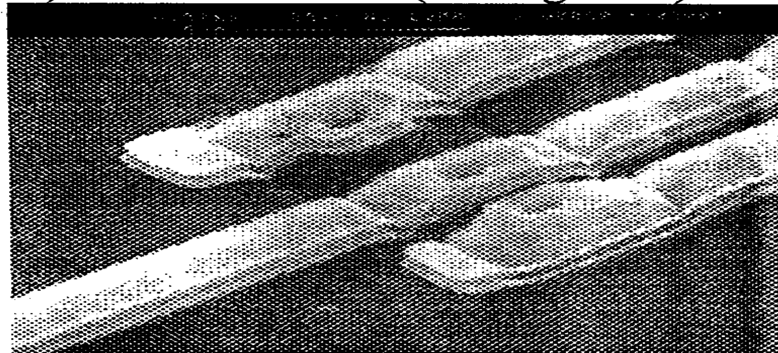

Figure 3. SEM photograph of buried silicide transistor NPN at metal 1.

Oxide dielectric and metal 2 was used to fabricate ring oscillators circuits.

3. Electrical evaluation

Fabricated buried silicide bipolar devices were assessed by looking at the DC electrical characteristics. Measurements of base-collector breakdown voltage were taken for each wafer to assess whether the vertical distance between the buried silicide (with its buried collector N+ implanted region) and the base region was adequate. This collector-base distance is determined by the grinding and polishing carried out after bonding of the silicided material. These were compared to the original FTIR measurements in table 1. From the table it can be seen that good breakdown voltages are seen.

Table 5.1. Table of breakdown voltages and FTIR measurements for buried silicide NPN devices.

Wafer	BVceo (V)	BVcbo (V)	FTIR Thick-ness (µm)	FTIR Std Dev (µm)
a	11.0	24	1.65	0.20
b	9.5	22	1.32	0.16
c	10.5	25	1.48	0.14
d	9	19	1.72	0.20
e	7.6	17.0	1.64	0.27

An example of a Gummel plot for a NPN with 0.75 x 12.5µm emitter is shown in figure 4 which show good linearity in beta over many decades of collector current.

At Vbe voltages of over 1.1V we see on the Gummel plots that Ib starts to rise quite rapidly. This leads to the rapid drop in beta above 1mA. This is not thought to be due to the buried silicide (which measures less then 1 ohm / square) but due to the 4 ohm cm silicon that was used as the active wafer in the bonding of the silicide. This replaces the N type epitaxy usually used in the fabrication of bipolar devices which is normally of much lower resistivity (~0.1-

0.3 ohm cm) and so higher doping level. This non-optimum active layer has the effect of increasing the device collector resistance.

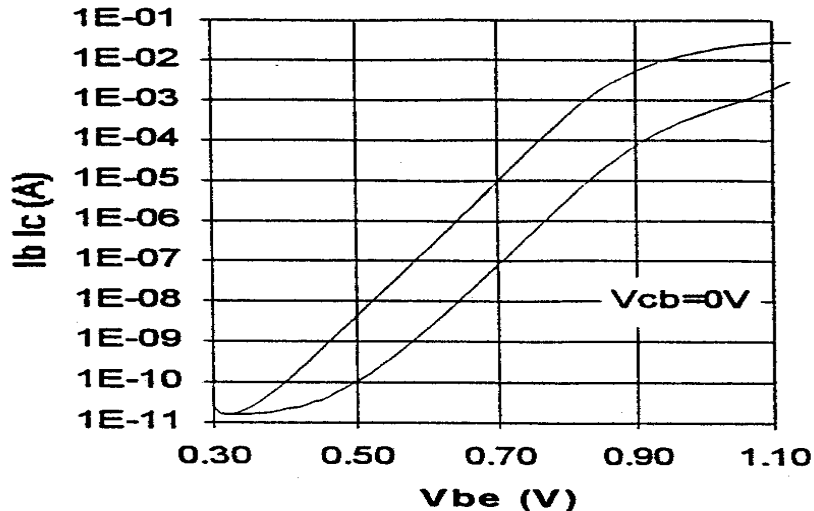

Figure 4. Gummel plot of 0.75x12.5 μm NPN on buried silicide at Vcb = 0V.

It was noted that the quality of the transistors have not been degraded by the incorporation of a buried silicide. In fact, an improvement in leakage and yield over devices on the standard bonded SOI material [5] was found. However, although it is possible that the buried silicide has reduced damage, it is far more likely that the modifications to the trench and field oxide were responsible.

An alternative bonded buried silicide on SOI, formed from sputtered tungsten, has been shown by cv plotting to be of good intrinsic quality [6] strengthening the validity of this class of material and may additionally act as a gettering site [7].

The f_T of the buried silicide NPNs were assessed and a typical plot is shown in figure 5 where the peak f_T is 5.6GHz at Vce of 2V and a collector current of 0.6mA. We would expect this device to peak at 1 to 2mA and modelling indicates that the higher effective collector resistance

has been caused by the high resistivity silicon.

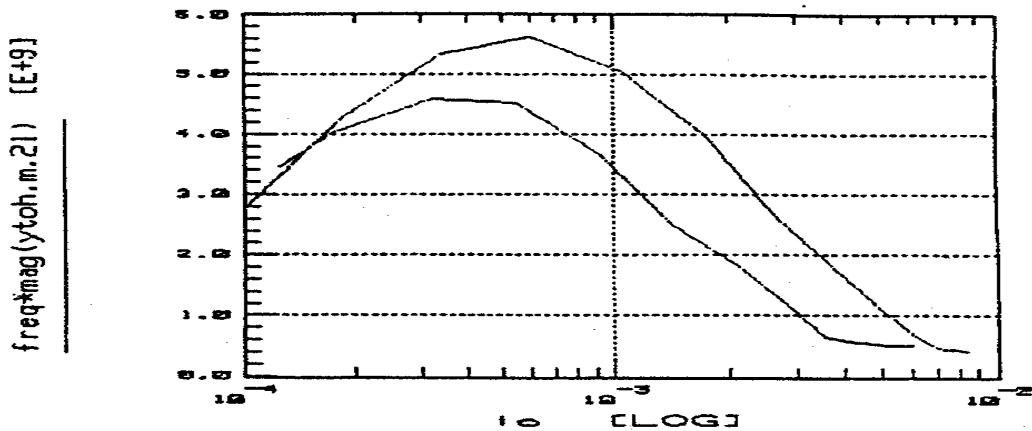

Figure 5. f_T plot of 0.75 x 12.5 μm emitter NPN on buried silicide.

Transistor to transistor breakdown voltage was checked on a curve tracer and was found to be greater than 150V, showing that the buried silicide had been completely etched through by the trench etching.

Circuit functionality was demonstrated by 41 stage CML ring oscillators as shown in figure 6.

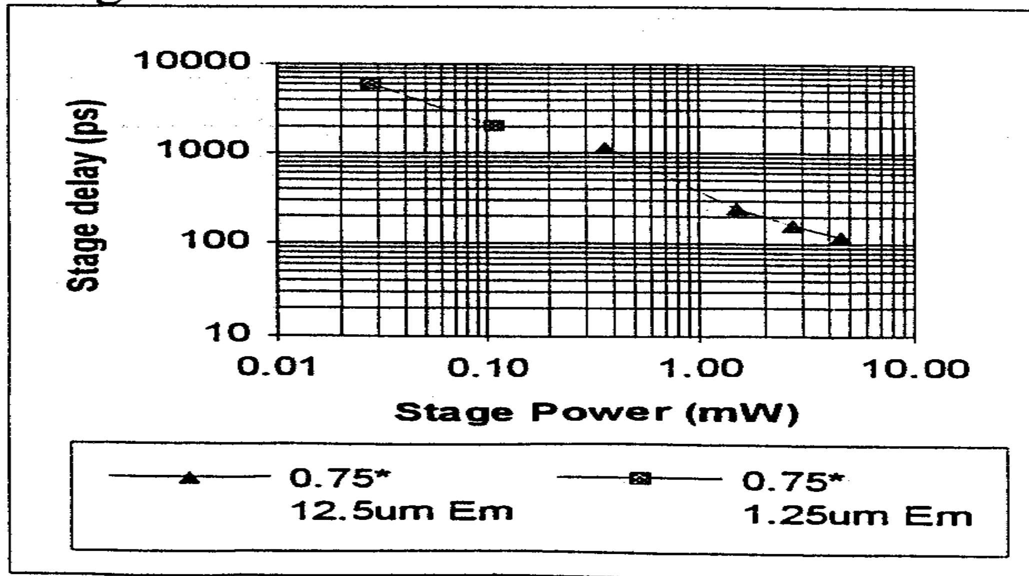

Figure 6. Ring oscillator power delay.

4. Summary

The electrical results presented show that the buried silicide SOI presents a viable process module that is compatible with high speed bipolar. This has the potential to provide a very low resistance collector to the NPN transistors though the use of higher resistivity active silicon than normal epitaxy has limited maximum speed.

The buried silicide appears to be compatible with the TEOS trench fill used. In fact, the TEOS trench fill, in combination with a lack of oxidation, has probably resulted in far less stress being formed around the trenches compared to non-silicide SOI [5]. This has resulted in NPN devices with good linearity.

We have seen from the electrical evaluation that the buried silicide has been successfully etched to give excellent isolation of devices at very high device-to-device breakdown voltages.

Thus it has been possible to see good NPN transistor action with no discernible harmful action by the silicide. Fully integrated processing with two layers of metal has allowed ring oscillators to be evaluated and demonstrate circuit functionality. Maximum f_Ts of 5.6 GHz have been observed which compliment the observed collector base breakdown voltages of about 17 - 25 V. These f_Ts are a function of the final effective collector - base distance and the resistivity of the active silicon layer (4 ohm cm). The collector - base is dictated by the thickness control of the mechanical grinding of the bonded active silicon film above the silicide layer. To thin this film thickness and improve thickness control, selective plasma thinning (PACE) has been used to fabricate material.

This, in combination with an optimised resistivity active layer, would enable the full potential of high speed bipolar to be realised on S^2OI..

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5. References

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