Control of Crystalline Defects in Trench Isolated Thick Film SOI for High Voltage Smart Power ICs

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ABSTRACT

We have studied the impact and control of trench related crystalline defects on thick film SOI for high voltage smart power ICs as well as those related to the wafer growth method, and evaluated their effects on device and circuit performance. We found that the deep trench etch coupled with the stress generated by the TEOS trench liner and polysilicon refill is the main source for creating crystalline defects such as slip dislocations. We also found that the doping level of the buried layer implant is an important contributing factor, while the trench profile also plays a role in slip generation. Careful optimization of the buried layer doping level and trench oxide liner thickness, and strict control of the trench profile is necessary to minimize the crystalline defect level and to achieve the desired electrical parameters. The choice of CZ and FZ wafers has a major impact on the surface defect density. In addition, the buried layer acts as an internal gettering layer to improve the minority carrier surface lifetime.

INTRODUCTION

Fusion bonded Silicon-on-Insulator (SOI) is gaining increasing attention as a substrate for high-voltage applications in areas such as telecommunications, displays and smart power (1,2). Trench isolated SOI offer higher packing density, much lower wafer bow/warp values and lower crystalline defect density than conventional DI (Dielectric Isolation) substrates. We have successfully manufactured and commercially supplied High Voltage (HV) Smart Power ICs using trench isolated thick film SOI wafers (BCO substrate[1]) with a 500V BCD (Bipolar-CMOS-DMOS) process (500V DIMOST[2]) for the first time. The use of trench isolation ensures >500V dc isolation for single trenches and >800V dc isolation for double trenches between adjacent components. A highly doped buried layer, together with trench sidewall doping guarantees small specific on-resistances for HV DMOS devices and prevents back gate assisted latch-up and punchthrough. The process combines DMOS and a wide variety of MOS and bipolar

[1] The BCO substrate is supplied by Analog Devices Belfast; it is trench etched and refilled SOI with or without buried device layer implant and doped trench sidewall.
[2] The 500V DIMOST process is a joint development of X-Fab Semiconductor Foundries and alpha microelectronics.

devices on the same die, and allows the configuration of circuits which are not possible or exhibit lower performance in junction isolated or thin SOI systems.

One of the major challenges in the manufacturing of crystalline defect free substrates for HVIC is that in order to realize the high voltage isolation required, the thickness of the liner oxide along the trench wall has to be increased. This causes an increasing level of tensile stress applied to the trench sidewall by the oxide layer. This tensile stress seems to peak near the trench bottom corner, and may eventually cause the generation of slip dislocations when the stress exceeds the yielding strength of the material (2,3). The buried layer implant appears to lower this yielding strength of the material at the trench bottom, thus making the substrate more susceptible to slip dislocation along the trenches for the same trench liner oxide thickness (4).

We have also examined the difference in using Czochralski (CZ) or Float Zone (FZ) wafers as the SOI device layer material. Bulk silicon wafers grown by the CZ method rely on denuding techniques to purge the oxygen from the surface device region in order to prevent the generation of oxygen precipitates and oxidation induced stacking faults (OSF). However, this denuding technique is not effective for SOI substrates (5,6). After studying the defect density when using CZ and FZ wafers as the device layer for this particular HVIC substrate, we decided that FZ wafers have to be used to reach an acceptable level of defect density.

PROCESS

Fig.1 is a schematic drawing of the trench-isolated SOI wafer. The device wafer received a blanket N+ implant before bonding. This implant is referred to as the buried layer implant. After bonding the device wafer to an oxidized handle wafer and thinning the device layer to the desired thickness, the wafer is trench isolated using an inductively coupled plasma (ICP) etcher. The trench sidewall is subsequently doped with phosphorus. After doping, the trenches are lined with a layer of LPCVD TEOS and filled with polysilicon. Finally, the wafer is planarized using a chemical mechanical polishing (CMP) technique and a layer of CVD TEOS oxide is deposited to protect the substrate surface, especially the top of the trenches. If the trench tops are not protected, then subsequent thermal oxidation steps will cause severe slip dislocations along the trenches.

The introduction of a buried layer implant not only lowers the Ron of HV DMOS transistors and prevents back gate assisted latch-up and punchthrough, but also has the added advantage of acting as an internal gettering layer to improve the surface lifetime and to enhance the gate oxide integrity (1,5,6). The deep trench etch is realized by using a one-step etch technique (7). To achieve such a deep trench etch without undercutting at the silicon and buried oxide (BOX) interface is a non-trivial task. The undercutting not only is a reliability concern due to oxide thinning but we also found that it contributes to crystalline defects such as slip dislocation generation. Fig. 2 shows the profile of such a deep trench with little undercutting at the silicon and BOX interface. The phosphorous doped trench sidewall together with the buried layer implant provides the low Ron required for DMOS transistors. However, this sidewall doping also increases the

likelihood of slip dislocation generation. Thus, its sheet resistance level has also to be carefully optimized to avoid the occurrence of slip dislocations.

The devices are then fabricated by a 2.5µm BCD process (500V DIMOST). The Power DMOS Transistor is the base component of the DIMOST. The device structure and the process parameters are optimized to obtain a drain breakdown voltage of greater than 500 V and maximum drain saturation current with a low on-resistance for the power DMOS. The electrical characteristics are dependent on channel length, drift-layer length, drift layer doping and extended-source field-plate effects. The specific on-resistance, RDS(on) x A, is typically 20 O.mm^2. The DMOS device is fabricated in a double-diffused process with a deep p tube to prevent secondary breakdown. The core process is chosen to form an optimized poly-gate n-channel vertical DMOS transistor; other process steps and masks have been added to integrate the CMOS part. The process utilizes single level poly, double level metal, self-aligned poly gates, ion implantation and dry etching of windows to form an optimized poly gate N-channel vertical DMOS transistor. This process allows the configuration of circuits which are not possible or exhibit lower performance in junction isolated or thin SOI systems. The monolithic integration of a full bridge rectifier with dielectric isolation enables easy reverse polarity protection, as well as higher efficiency. The additional integration of bipolar transistors allows the implementation of highly efficient driver circuits and improved reference elements. Cross-sections of the HV DMOS and CMOS structures are shown in Figs. 3 and 4, respectively. Typical device characteristics are listed in Table 1. The definition of VGS(th) is VGS=VDS at ID=1µA.

Table 1. Typical Electrical Parameters

Devices	500V DMOS	350V DMOS	300V PMOS	15V NMOS	15V PMOS
VGS(th) (V)	1.5	1.8	-0.5	1.0	-1.0
V(BR)DSS (V)	500	350	-300	>20	<-20
RDS(ON) (O)	10 - 900	400 - 2500	4000	-	-

Devices	80V NPN1	80V NPN2	450V PNP	200V PNP	80V PNP	20V PNP
ß	50	500	60	50	90	130
V(BR)CEO (V)	80	80	-450	-200	-80	-20
V(BR)CBO (V)	80	80	-450	-300	-150	-50

RESULTS AND DISCUSSION

Background

A 5'' DIMOST process based on 5'' conventional DI substrate had been previously used to manufacture HV smart power ICs. However, when the wafer foundry upgraded to a 6'' line, 6'' DI substrate proved difficult to source, and also had too high a bow/warp value to be processed. Thus, an alternative wafer substrate had to be developed to replace the DI substrate.

Trench Oxide Liner Thickness Optimization

The main factor influencing the generation of slip dislocation along the trench is the thickness of the trench sidewall oxide liner. If we define the thickness of this oxide liner at the on-set of the slip dislocation as Tsp, Tsp is a weak function of SOI layer thickness, dosage level of the buried layer implant, doping level of the sidewall doping, degree of trench undercutting at the silicon oxide interface, and the SOI layer material properties (4). Two SOI layer thicknesses, 30um and 50um were investigated initially, and from the results, the thicker SOI layer thickness of 50um was found necessary to meet the HV DMOS breakdown voltage requirement.

A highly conformal low stress LPCVD TEOS process is used for the trench oxide liner. A trench oxide liner thickness of 3.5kÅ on each sidewall was used initially, and although the substrate was slip free, it just about met the trench isolation voltage of 500V. Therefore, to reach the desired high dc breakdown voltage between adjacent components, the thickness of the trench sidewall oxide liner has to be increased accordingly. Silicon dioxide of thickness greater than 1000Å has a breakdown strength of approximately 8MV/cm (8). The breakdown strength of the densified TEOS used for the trench liner in our process is comparable to that of the thermally grown oxide. The increase of the trench oxide liner thickness causes an increasing level of tensile stress on the trench sidewall, which peaks near the trench bottom corner, and may eventually cause slip dislocations when the stress exceeds the yielding strength of the material. Thus, the slip dislocations usually begin to appear at the trench bottom corner, then propagate to the wafer surface along the <111> plane in the subsequent thermal process cycles. An example is shown in Fig. 5. We were able to deposit 5kÅ of the TEOS on each sidewall, which yielded a minimum level of slip dislocations (see Fig. 6) and met the >500V trench isolation voltage specification. To achieve the 800V trench isolation voltage specification required at some parts of the circuit, a thicker trench oxide liner is desirable, but the level of slip dislocations become unacceptable (see Fig 7). Hence, a comprise approach is necessary, in which the thickness of the TEOS liner of 5kÅ is chosen to satisfy the 500V trench isolation voltage specification, and double trenches are used for the parts of the circuit that require >800V trench isolation voltage.

Buried Layer Implant Optimization

The main reason for the introduction of a buried layer implant is to lower the Ron of HV DMOS transistors and prevent back gate assisted latch-up and punchthrough. As an added bonus, it also acts as an internal gettering layer to improve the minority carrier surface life-time (5,6). However, the downside is that it also lowers the Tsp. Thus, a balancing act has to be performed to meet the electrical parameter specification and to keep the degree of slip dislocation at a minimum level.

An implant dose of 1e16/cm^2 at 30keV was chosen initially. However, this implant dose coupled with the 5kÅ TEOS liner caused multiple slip dislocation lines to be seen along the trenches from the top surface, as viewed using Nomarski microscopy. When a lower implant dose of 3e15/cm^2 at 30keV was used, it was found that this only caused a very small Ron increase, but reduced the slip dislocations dramatically to an acceptable level (Fig. 6). Implant doses lower than 3e15/cm^2 at 30keV were investigated by process

and device simulation. The simulation indicated that any buried layer implant dose lower than 3e15/cm^2 at 30keV would make the Ron too high, and thus was unacceptable.

The conventional gettering methods used on the bulk silicon wafers, such as the formation of oxygen precipitates in the non-active area together with denuding of the active area, back surface etching etc., cannot be applied to SOI substrates (5,6). This is due to the fact that the BOX layer acts as a barrier for such techniques to be effective. However, we found that the buried layer implant acted as an effective gettering layer for the SOI substrate. The average surface minority carrier life-times of the substrate after SOI polishing and thermal oxide growth as measured by SCA (Surface Charge Analyzer) over a period of time are listed in Table 2 below. The typical SOI surface life-time of a comparable SOI layer material without the buried layer implant as measured by SCA is between 50 and 150µs. Thus, the beneficial effect of the buried layer implant on the BCO substrate surface life-time is evident due to its gettering effect.

Table 2: Average Surface Life-time (µs) as Measured by SCA

LOT ID	**LIFETIME (pt 1, flat)**	**LIFETIME (pt 2, center)**	**LIFETIME (pt 3, top)**	**LIFETIME (pt 4, left)**	**LIFETIME (pt 5, right)**
Lot 1	653	580	533	610	621
Lot 2	946	1285	1536	1433	443
Lot 3	596	425	791	657	338
Lot 4	681	395	401	468	744
Lot 5	442	435	656	325	458
Lot 6	549	573	607	437	849

Control of Deep Trench Etch Profile

Silicon undercutting at the silicon and BOX interface along the trench bottom, otherwise referred to as trench footing (Fig. 8), is undesirable not only from a reliability point of view due to possible TEOS thinning, but we also found that it plays some role in increasing the possibility of slip dislocation generation for the same liner thickness. Thus, the trench footing has to be kept to a minimum.

For such a deep trench etch, an ICP system is favored over an RIE (Reactive Ion Etching) system due to its high etch rate, its ability to etch high aspect ratios and its ability to control the trench profile, i.e. straight trench sidewalls without bowing. We initially used an STS (Surface Technology Systems) Advanced Silicon Etch (ASE) process, based on their Multiplex ICP system. However, this process cannot be used on SOI wafers due to the severe trench footing it produces (Fig 8). Therefore, we developed a two-step ICP and RIE compound process to circumvent this problem. Trenches were etched just short of the BOX layer to benefit from the ICP technology, then the etch was finished off by switching to RIE. However, this approach is not economical in production. By working with STS on an alternative approach, we have developed a one-step ICP deep trench etch based on their ICP ASE SOI module (7). This alternative process enabled us to minimize the trench footing (Fig. 9) thus reducing the possibility of slip dislocation generation, and eliminating the reliability concern. It also allowed us to have greater control of the trench profile, so that the trench sidewall could be tapered to a 88.5° angle, to help achieve a void free trench refill with polysilicon (Fig. 2).

Wafer Growth Method: CZ or FZ

Device layer wafers that were produced by different wafer growth methods, i.e. CZ or FZ, were also investigated. Bulk silicon wafers grown by the CZ method rely on denuding techniques to purge the oxygen from the surface device region to prevent the generation of oxygen precipitates and OSFs. However, this denuding technique is not effective on SOI substrates. We found that the choice of using CZ or FZ wafers had a major impact on the surface defect density. The CZ wafers were 10-20 O.cm, <100>, n type phosphorous doped. The FZ wafers were 23 O.cm, <100>, n type phosphorous doped. Both types of wafer were processed together through the AD Belfast and foundry lines. After the wafers were finished, the samples were prepared for analysis by polishing bevels to approximately 5°50, then the bevels and surface were etched with Yang etchant (2M CrO_3-Lsg. : HF (50%) =1 : 1) for 2.5 minutes at room temperature. A Nomarski microscope and an interference phase contrast microscope were used for observation of defects. Fig. 10 (a) shows the results for a CZ wafer sample, and Fig. 10 (b) the results for an FZ wafer sample. Both types of samples show a single line of slip dislocation along the trenches. In addition, 4e6 cm^{-2} of oxygen precipitates were observed on the CZ sample while no such oxygen precipitates were seen on FZ wafers. From our other studies (6), we conclude that this high level of oxygen precipitates occurs in the CZ device layer due to a high level of oxygen presence in the starting wafers. The oxygen concentration for the CZ wafers was specified at 7.5e17 +/- 1.0 At/cm³. We believe that the oxygen level needs to be controlled at a lower level such as <7e17At/cm³ to reduce the oxygen precipitate density to an acceptable level. Due to this advantage with respect to the surface defect density, plus the tighter resistivity control over CZ wafers, FZ wafers were chosen as the device layer material for this HV smart power IC product family.

Electrical Parameters Evaluation

All the main electrical parameters are comparable to the original DI substrate for the BCO substrate. The bow of the 6'' BCO substrate is low after the completion of the DIMOST process (<50µm) compared to the DI substrate. The crystalline defect density is much lower than the conventional DI substrate. The single line slip dislocation along the trenches had no adverse effects on the device and circuit performance. A minimal feature HV DMOS electrical characteristic is shown in Fig. 11.

CONCLUSION

In this paper, we have successfully manufactured and commercially supplied High Voltage Smart Power ICs using trench isolated thick film SOI with a 500V BCD process for the first time. The impact and control of trench related crystalline defects, as well as those related to the wafer growth method were studied, and their effects on device and circuit performance evaluated. We found that the deep trench etch coupled with the stress generated by the TEOS trench liner and polysilicon refill is the main source for creating crystalline defects such as slip dislocations. We also found that the doping level of the buried layer implant is an important contributing factor, while the trench profile also plays a role in slip generation. Careful optimization of the buried layer doping level and

trench oxide liner, and strict control of the trench profile is necessary to minimize the crystalline defect level and to achieve the desired electrical parameters. The choice of CZ and FZ wafers has a major impact on the surface defect density. In addition, the buried layer acts as an internal gettering layer to improve the minority carrier surface lifetime. We found that a single line of slip dislocations along the trenches has no adverse effects on the device and circuit performance. Further work is being carried out at the moment to develop an alternative process flow to make the BCO substrate completely free of crystalline defects with a thicker trench oxide liner for the HV smart power ICs. This will allow a tighter design rule and the elimination of double trenches, and offer even higher packing density.

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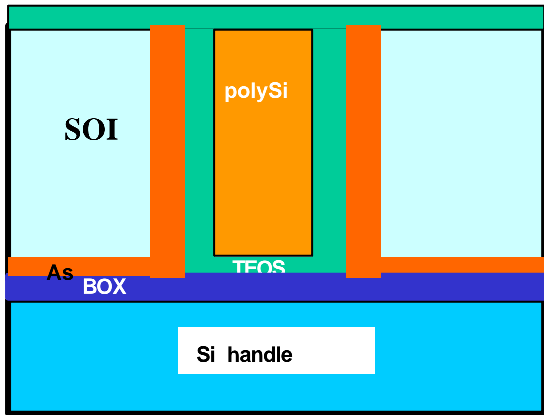


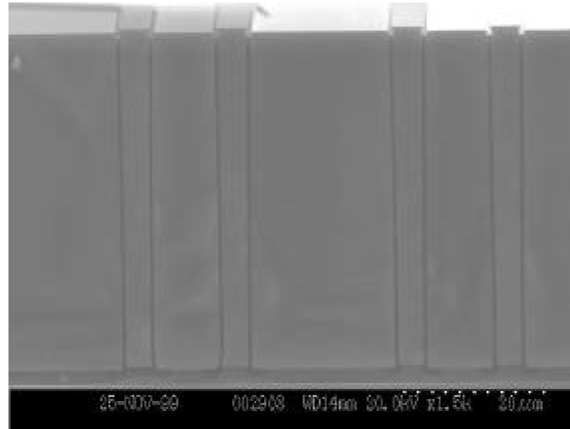
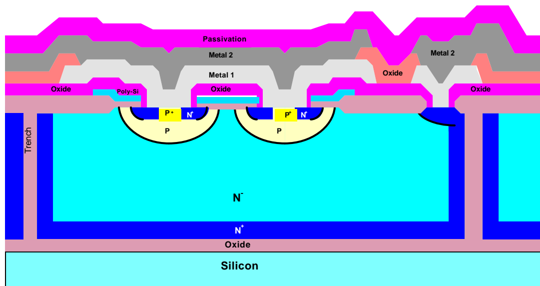


Fig.1. Schematic drawing of the trench isolated SOI wafer

Fig. 2. Profile of a 50 um thick deep-trenched SOI wafer without undercutting of silicon at the trench bottom



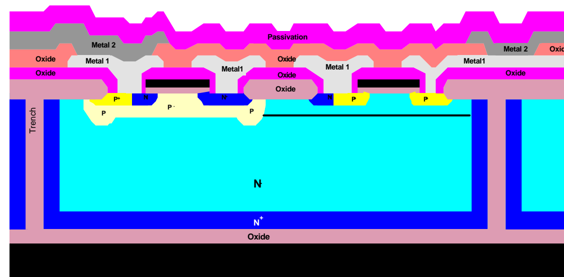
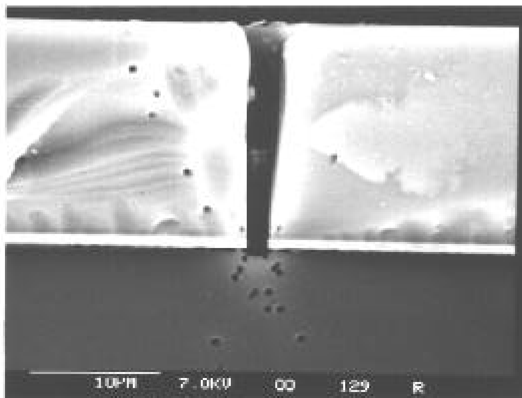


Fig.3. Schematic drawing of the cross-section of the HV DMOS

Fig.4. Schematic drawing of the cross-section of the CMOS



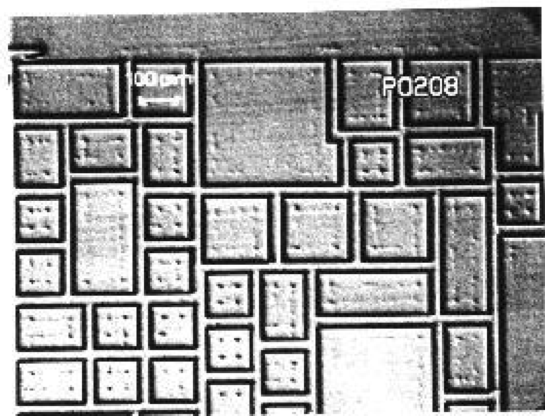


Fig. 5 Example of a defect etched cross-section of a trench with single line slip dislocations

Fig. 6. Single line slip dislocations along the trenches viewed through a Normaski microscope after defect etch

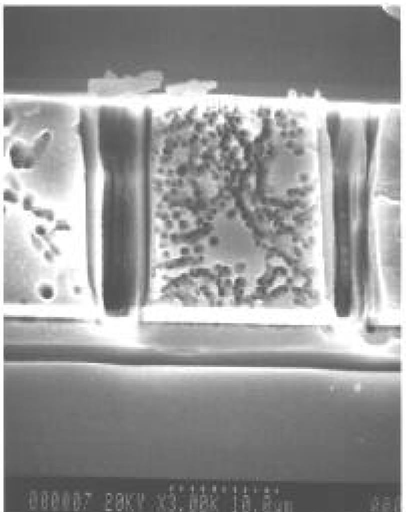


Fig. 7. Example of a defect etched cross-section of a trench with a high level of slip dislocations

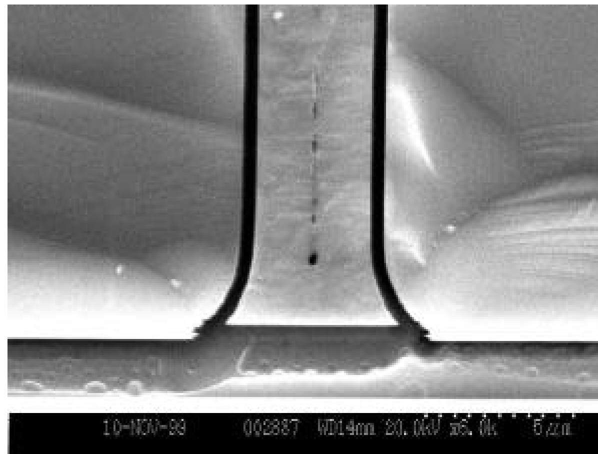
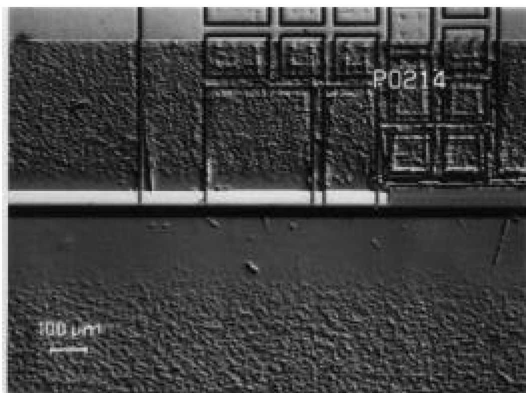


Fig. 8. Example of trench footing



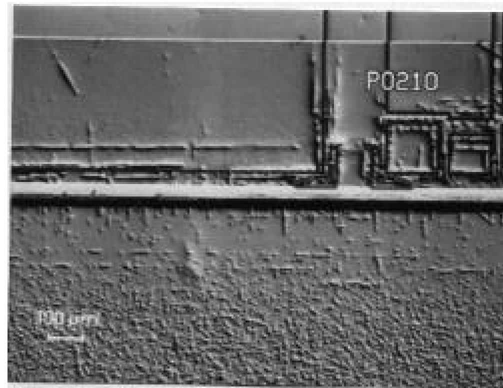


Fig. 10. Surface defect density of SOI using (a) CZ and (b) FZ wafers for the device material

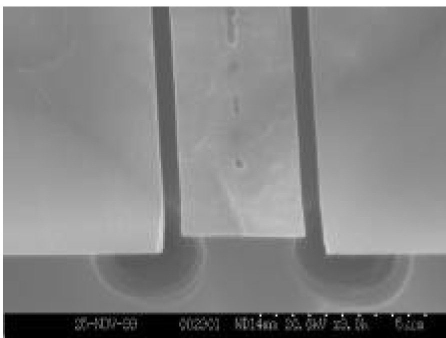


Fig. 9. Profile of a deep-trenched SOI wafer with minimum undercutting of silicon at the trench bottom

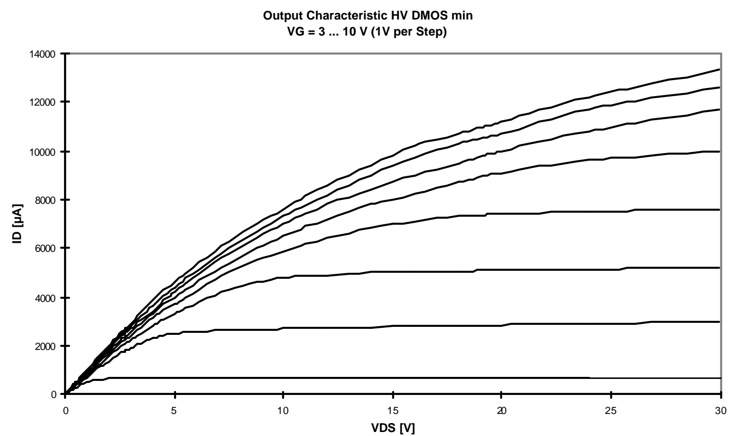


Fig. 11. Electrical output characteristics of the minimal HV DMOS transistor.
Important electrical parameters are
Drain-to-Source Breakdown Voltage: V(BR)DSS > 500 V
Gate-to-Source Threshold Voltage: VGS(th) = 2 V
Static Drain-to-Source On-Resistance: RDS(on) < 1000 Ohm