Physics and Applications III (ECS Proceedings series, PV 95-7, Pennington, NJ,1995),56

Mechanical Thinning for SOI

by

Dr. Scott Blackstone BCO Technologies

Mechanical thinning now totally dominates the fabrication of SOI wafers with film thicknesses above one micron. Continued advances in this technology could potentially allow the fabrication of TFSOI layers by purely mechanical means.
Current state of the art techniques for mechanical thinning of SOI wafers are reviewed. These include both equipment and measurement issues. Particular emphasis is placed on the manufacturability of these techniques.

The remarkable progress in the mechanical thinning of SOI material is a direct result of the parallel efforts in unrelated areas. Specifically, the two areas that have been of greatest significance are one, the push to O.3m wafers and the requirements of large random logic IC for four or more levels of interconnection. The first has created a new and large market for ultrahigh precision grinding while the second has almost totally revolutionized the field of polishing technology. As a result of these commercial developments, several SOI manufacturers worldwide are currently able to provide thickness uniformity specifications of +/-0.5um using purely mechanical means. It is expected that in the next five years this can be reduced to +/-0.2um with a longer term expectation that mechanical thickness control will be the technology of choice for all SOI applications.

Grinding Technology

Grinding is now replacing lapping in the manufacture of the next generation of bulk silicon wafers. The principle advantages of grinding over lapping are tighter control over mechanical dimensions and lower sub-surface damage. It is now believed by most manufacturers of silicon wafers that some form of grinding technology will be required to meet the requirements of the JESSI/SEMATECH roadmap for O.3m wafers. As a result, the wafer manufacturers have created a new demand for ultra high precision grinders. A number of grinder manufacturers have responded to this demand creating a new class of grinder almost ideally suited to the manufacture of SOI wafers by mechanical thjnning [1,2,3].

The requirements of the SOI community and the wafer manufacturers are similar I but they are not identical. The areas where there is the greatest agreement is in TTV (Total Thickness Variation), or what is sometimes called flatness, and sub-surface damage. Both communities are working toward a TTV and subsurface damage goal of zero. Both parameters are important because they translate into SOI film thickness uniformity. Typically, any operations after grinding, such as etching and polishing, degrade the flatness achieved by grinding and therefore have to be minimized. The final TTV of a wafer is the TTV after grind degraded by a constant times the depth of sub-surface damage.

The area where there is the greatest difference between the SOI community and the wafer manufacturers is in absolute thickness control. The SOI community require an absolute thickness control that is one hundred times greater than the bulk silicon wafer manufacturers. Bulk wafers have an absolute thickness control of +/-15urn, whereas SOI manufacturers require +/-0.15urn, or better. Even worse, the SOI community measures TTV as thickness deviation from an absolute value whereas the wafer manufactures measure it in a relative manner as long as the absolute thickness is within the +/-15 urn specification (Fig 1).

The importance of absolute thickness control is shown in Fig 2. First an ultraflat wafer of known thickness, called the handle wafer, is bonded to a device wafer . Then the device wafer is thinned using the back of the handle wafer as a reference. It is important to point out that the wafer is thinned to a total thickness and not an SOI layer thickness as shown in Fig 2. From the mechanical thinning point of view, the SOI layer thickness is the total thickness minus the handle layer thickness. This is commonly referred to as backside referenced as opposed to, for instance, etch stop technology which is front side referenced. All grinding technology is backside referenced.

Grinder Configurations

Creep Feed

Traditionally, silicon wafer grinding was the domain of IC manufactures for thinning the finished wafer to meet packaging height requirements. The technology that was widely used for a number of years was creep feed grinding. In this configuration, a grind wheel is set at a predetermined height and the wafer is feed laterally under the wheel. One of the principle disadvantages of this approach is that the cut depth is limited and as a result multiple passes are needed. Multiple passes are typically achieved by using multiple spindles which adds to the capital cost. In addition, creep feed grinders suffer from deep damage that is believed to be due to the deep depth of cut required for economic throughput [4].

In-Feed

Creep feed grinding has been largely replaced by in-feed vertical grinding (Fig 3). In this configuration, the wafer is placed on a rotating chuck beneath the grind wheel. The grind wheel is positioned so that the center of the cutting blade is over the center of the wafer .The grind wheel cuts from the center to the edge in a thin slice. The grind wheel is then feed vertically down into the wafer allowing it to cut to any depth with a single grind spindle.

This approach has a number of advantages over the creep feed method in addition to the need for fewer spindles. The cut length of the in-feed is constant and thus the load on the spindle is constant as opposed to the creep feed in which the cut length starts at a minimum, increases to a maximum in the center and then decreases back to a minimum again as it exits the wafer .However the principle advantage of the in- feed system is that the depth of cut is very small.

Using typical grinding conditions, the depth of cut for an in feed grinder (Feed rate/wafer rpm) is one hundred times less than for a creep feed grinder (O.lum vs lOum). This very low depth of cut results in low sub-surface damage as well as low surface roughness [4]. In-feed grinding has another important advantage for the SOI community, which is in-situ thickness control. Because half of the wafer is always exposed during grinding, it lends itself to the use of stylus type measurement of the wafer thickness during grind to obtain a closed loop control of thickness.

Single Point Diamond Turning (SPDT)

SPDT is widely used for the manufacture of contact lenses and germanium optics for m applications. It is a technique in which a natural single crystal diamond is shaped into a wedge like point with a tip that is only a single atomic line and is used to "shave" material off the surface. The principle advantage of this technique is that it produces both a very smooth surface as well as an extremely low depth of damage because it works in the "ductile" mode. Surfaces as smooth as Inm (Ra) and damage as shallow as 0.4 um have been reported [5,6,7,8,9]. No data has been reported on damage distribution within a wafer or on the TTV's achieved using SPDT .

SPDT has one very significant drawback that will continue to limit its application which is diamond wear .For reasons that are not totally understood. silicon has a tendency to wear the diamond tool at a very high rate. Most researchers find it difficult to machine even a single wafer without leaving a isolated deep damage scratch on the wafer as a result of diamond wear .

Horizontal Type Ultraprecision Grinder

The Horizontal Type Ultraprecision Grinder [3,8] configuration is shown in fig 4. This grinder uses a solid grind wheel that cuts across the wafer in a spiral much like the grooves of a record. The principle advantage of this configuration is mechanical stiffness. The solid grind wheel can be held more accurately than a cup wheel which flexes during grinding. This configuration is particularly interesting to wafer manufacturers because the throughput is independent of the depth of cut.

No TTV or damage distribution data has been published on this configuration. Depth of damage in the order of 1-1.5um in the center with a RMS surface finish of 25nm [8,9] has been reported. This damage is quite low for this type of grinding considering its very deep depth of cut. If this damage is uniform across the wafer , while achieving a submicron TTV, then this technique holds great promise for the future.

Discussion

Any discussion of grinding technology must include a discussion of measurement tools and techniques. In particular, the measurement of thickness and depth of damage. Currently only one tool is capable of measuring wafer thickness with high accuracy. This is the range of wafer measurement tools by ADE Corp [10] with their E-station or enhanced E-station gage.

Depth of damage is measured by a number of techniques and it is important to know which ones are used as they all give differing results. The most common technique is the angle lapping and staining of a ground surface. This technique can measure submicron damage but is confined to a small area. Even lower levels of damage can be measured by cross sectional TEM but this is confined to an even smaller area. Because damage distributions are frequently not uniform across the wafer , it is important to make several measurement across the wafer and to identify where on the wafer these measurements were taken.

Finally, the worst case damage technique is to remove a series of thin layers from the entire surface of the wafer until all of the damage is removed. The depth at which the wafer is totally defect free is then the depth of damage. This technique is. ideal for identifying small scratches or other artifacts of a grinding process whose density would be to low to be detected by other techniques. From a wafer manufacturing point of view, one tiny scratch three microns deep on a wafer with an otherwise uniform submicron damage layer is equivalent to a wafer with a uniform damage layer three microns deep. The removal of the thin layers is typically accomplished by polishing a series of wafer to different depths immediately after grinding and then etching the wafer with a defect etch [11]. A new technique for mapping damage was recently proposed based on depolarization of infrared light (SIRD) which allows the creation of damage maps on a single wafer [12]. This technique is currently limited by its depth resolution of one micron but shows great potential as an in-process control tool.

Today, all SOl manufacturers use in-feed grinders for the grinding of SOl wafers. Currently the most widely used grinder is the Shibayama VG-202 [1]. This grinder achieves submicron TTV's in a production environment. The absolute thickness control on this machine is +/-lum.

Some of the lowest TTV wafers ever reported have been ground on an in-feed grinder. Fig 5 is an example of a wafer ground on a VG-202 in a production environment showing the ability to achieve deep sub-micron flatness. The principle limitation on

TTV is spindle stiffness. Most TTV loss on wafers with flats occurs at the flats as a result of the load change on the spindle. Advances in spindle bearing design such as electrodynamic spindles using active controls show promise of higher stiffness than conventional air bearings.

Currently the two largest limitations to the in-feed grinder are the total thickness control and the worst case depth of damage. A total thickness control of +/-lum is the result of current sensor limits using a stylus gage and are not the inherent limitations of machine design. While this control is acceptable for handle wafer formation, it is totally unacceptable for SOI wafer formation. New and better thickness control techniques are required.

Depth of damage on the in-feed grinder is a function of radial position. The lowest damage is in the center where the relative movement of the wafer against the grind wheel is low. The maximum damage is at the edge of the wafer where the relative movement is the largest. Using a grind wheel with a diamond size in the order of a few microns produces sub-micron damage in the center of the wafer but damage at the edge of the wafer can be 2-4 times deeper.

Electrolytic dressing has been proposed as a technique of achieving lower depth of damage using in-feed grinding [13,14]. In this technique the material that holds the diamonds in place is eroded electrochemically. By controlling the erosion rate and thus the supply of "fresh" diamonds, it potentially allows the use of diamond wheels that are too fine to use otherwise and as a result obtain a lower level of damage.

A new type of grind wheel abrasive called Ultrafine Abrasive Particle Grinding (UAPG) has been proposed [2]. This grind wheel uses silica particles O.Ol-O.O2um in diameter instead of diamonds. Submicron damage in the center of the wafer has been reported but no data exists on the distribution of the damage. The surface finish reported was significantly better than conventional diamond wheels. The best case surface finish, Ra of 1.4nm is almost comparable to a polished surface.

Polishing

Traditionally, polishing is simply a means of planarization. After grinding, the damage is removed by chemical etching which leaves a rough but damage free surface. This surface is then planarized using polish technology to achieve a smooth surface. However I in SOI, polishing plays a second equally important role and that is thickness control. While grinding sets the TTV or flatness, polishing sets the thickness of an SOI wafer .

Wafer manufacturers typically uses multiple wafer polishers because they offer low capital cost while at the same time achieving a high degree of flatness. However , these polishers have very poor absolute thickness control within a batch and are therefore not usable for SOI manufacturing. To achieve thickness control, the SOI community has turned to the single wafer polishers that have been developed for the IC community to achieve planarization of multiple levels of metallization within an IC [15,16,17,18,19 I. These machines are typically referred to as CMP (Chemical Mechanical Polishers) tools. Unfortunately, most of these machines have no characterization data for silicon polishing what so ever and it up to each SOI manufacturer to develop its own process.

While the single wafer polishers can offer excellent thickness control across a lot of wafers, the individual wafer TTV control is more difficult. The principle mechanism for TTV loss is the formation of a wedge in the wafer shape. This wedge formation is typically caused by the inability of the chucking mechanism to apply pressure to the wafer without restricting the wafer's ability to follow the contours of the pad. A great deal of progress has been made in the ability to build low effective mass wafer chucks in the newest state of the art CMP machines. An example of just how far this design has 'developed is shown in the chuck design of the Cybeq Isoplanar 7000 [Fig 6] [17]. Here, the effective mass of the chuck has been reduced to the wafer itself and a thin ceramic carrier which is then suspended on a cushion of air, decoupling the rest of the chuck while providing the necessary down force.

Another feature of the latest CMP machines is the degree of automation that is readily obtainable. This means that it is possible to couple the pre-polish SOI thickness data of each wafer into the polisher so that adjustments can be made to automatically achieve a uniform thickness. A recent machine from Presi [19] for instance can have all of the measurement and automation necessary built right into the tool.

A polishing process in which the wafer is rigidly held has been proposed by BCO Technologies and others[20]. This approach, called In-Feed Vertical Polishing, uses the same configuration as an in-feed grinder except the grind wheel is replaced by a polish pad [Fig 7]. In this configuration, because the wafer is rigidly held it is impossible to form a wedge in the wafer. Fig 7 is the ADE plot of a wafer polished using this technique. The thickness control is +/-110nm with no wedge formation.

This in-feed polishing has two important advantages for SOI applications. Because half of the wafer is always exposed during the polishing, it is possible to use in-situ thickness measuring tools during polish of an SOI wafer as an end-point. This means that thickness control can be independent of temperature, pad conditioning, slurry, etc. The second advantage is that it allows the formation of handle wafers without grinding. Standard polished, or lapped and etched, wafers can be polished directly on the in-feed polisher to a high degree of flatness directly without grinding first.

Thin Film SOl

The above polish techniques are currently limited to SOI films that are one micron or greater in thickness. To produce films in the thickness range of 0.1 micron requires alternative approaches. The two approaches that have demonstrated results are small tool polishing and polish stop technology .

Small Tool Polishing

Small tool polishing is a widely used technique for making large optical components. In this technique a polish pad mounted on a rotating tool much smaller than the wafer being polish is moved across the wafer by numerical control to achieve the desired shape. In this case, a multi-micron SOI layer is first mapped for thickness. Then a very small diameter polish pad is moved across the surface of the wafer varying dwell time inversely to the thickness of the SOI layer. After a series of passes, the SOI layer can be make completely uniform [21].

This technique has not been widely adapted because of throughput. The effective removal rates of this technique are very low and as a result it can take an unacceptably long time to thin a wafer from a nominal 3um to 0.lum. In theory however this technique would not be restricted to a single polish head or a single polish head diameter .

Polish Stop Polishing

The only mechanical approach that has been demonstrated to achieve absolute thicknesses in the order of O.O8-0.1um with a 1TV of l0nm or less is the polish stop approach [22,23,24,25,26]. The polish stop approach works by predefining a pattern onto the wafer with a material which polishes at a much lower rate than the silicon thus locally stopping the polishing. One such polish stop approach is shown in Fig 8. This approach is what might be terms "LOCOS before Bond" in that the LOCOS oxide is grown before bond and acts as a polish stop. In addition to thermal oxide, other polish stops have also been reported such as SiC, BN, SiBN, Si_3N_4 and Al_2O_3 [27,28].

In this technique of LOCOS before bond, the LOCOS thermal oxide is formed on the device wafer first. This device wafer is chosen to have the correct resistivity 1 orientation and doping as required by the final CMOS process. The LOCOS oxide is covered by a thick CVD oxide layer which is then smoothed sufficiently for bonding. A handle wafer is then bonded to this CVD oxide and the device wafer is ground to within a few microns of the top of the LOCOS stopping oxide. Finally, the wafer is polished with a process optimized to stop on the LOCOS oxide layer. This leaves single crystal islands that have the same thickness as the LOCOS oxide thickness.

Using the technique of Fig 8, one research group [29] has reported a TTV of 8nrn on a 6" wafer with a film thickness of 60nm. This film thickness control is comparable to the best of SIMOX or BESOI. The principle advantage of this approach is that it offers the crystal quality of bulk silicon. The disadvantage of this approach is that it is an application specific wafer and not a techniques for producing commodity products.

In addition to crystal quality this approach has a number of other advantages over SIMOX and BESOI. This approach leaves a perfectly planar surface as the active area is already defined by the polish stop process. The biggest advantage however is the ability to pre-process the wafer prior to bonding. The greatest focus on preprocessing prior to bond has been in two areas. The first is the ability to put a polysilicon gate on both top and bottom of the transistor to achieve higher drive current per unit area [29130,31]. The second is the ability to make a backside ohmic contact to the body of the transistor and thus control its potential [32,33].

Future Development Path

Over the next five years, the mechanical thinned SOI product range will diversify to satisfy the various price performance needs of the marketplace. This diversification is outlined in Fig 9. It is predicted that state of art mechanical thinning technology will continue to achieve higher and higher levels of accuracy but that "fallout" technologies will allow a trade off between cost and thickness accuracy. The range of thickness accuracy offered will be from +/- lum to +/-0.01 urn with a corresponding cost variation from 3X wafer cost to lO X wafer cost.

Currently, the manufacturing of SOI material by mechanical thinning is restricted to offering a single specification of +/- 0.5um. This is in spite of the fact that several applications would benefit from a lower cost with a specification of +/- 1.0 um. The reason for this is that higher throughput grinding and polishing tools simply could not meet a thickness specification of +/- 1.0 um.

It is predicted that the first major trend toward diversification will come in the area of high throughput, high accuracy grinding technology .Many of the developments in the manufacture of ultrahigh precision grinders for SOI applications can be applied to the high throughput grinders developed for IC back-grinding applications. These upgraded back-grinders would then be able to grind wafers to a near-submicron specification allowing the lower cost fabrication of SOI wafers with a thickness specification of +/- 1.0 um.

The accuracy of grinding and polishing SOI material will continue to improve to the point where thickness control of +/-0.25 urn will be routinely achieved. This improvement will come from a gradual improvement of existing technology .

At this point the market will offer two products. One will be an SOI wafer with a thickness specification of +/- lum at 5x wafer cost and the other will be an SOI wafer will a thickness specification of +1- 0.25 urn with a lO X wafer cost. This will create a new market opportunity for a lower cost SOI wafer with a thickness specification of +/- 0.5 urn particularly for the Bipolar marketplace.

Because of the differing demands of the low cost SOI marketplace, the +/- 1.0 urn SOI wafers will further diversify into a very low cost +/- 1urn specification for the sensor marketplace (Sensor Grade) and a low cost +/- 0.5 urn SOI wafer for the bipolar marketplace (Bipolar Grade). The Sensor Grade will be offered at 3X wafer cost while the Bipolar Grade will be offered at 5X wafer cost. The Bipolar Grade material will be achieved by post-processing very low cost SOI wafers using in-feed polishing.

Mechanical thinning technology will probably achieve a diminishing level of return at an accuracy level of+1- 0.1 urn. Wafers with this degree of control, named CMOS Grade, will only cost BX wafer cost because of improvements and large market demand. This level of thickness control will satisfy an but the fully depleted CMOS applications.

To achieve the degree of thickness control for fully depleted CMOS, or the so called TFSOI, the CMOS Grade wafers will be post-processed using small tool polishing or the CMOS Grade technology will be combined with selective polishing.

This concept of post-processing lower cost, higher volume SOI products will continue into the future creating a wide variety of product offerings. This will be possible because the cost impact of post processing will be minimized by the very small amount of material removal that will be required.

Conclusion

Mechanical thinning of SOI has made rapid progress in the last several years. This is the result of silicon wafer manufactures pushing the state of the art in grinding technology and IC manufacturers pushing the state of the art in polishing technology. As a result of these developments, thick film SOI wafers can now be routinely made with a thickness specification of +/-0.5um. Newer developments will continue to push this tolerance tighter .Using small tool polishing or oxide polish stop technology, thin film SOI layers can be achieved with thickness tolerances comparable to any other thin film SOI approach.

Acknowledgement:

I would like to acknowledge in particular the help of Dr. P. Hahn of Wacker in preparing this paper. In addition I would like to acknowledge helpful discussion with Mr. Iida of Shibayama, Mr. R. Nagahara of Cybeq Systems, Mr. R. Wells of Motorola, Dr. v. Nayer of DRA/UK, Dr. T. Abe of SEH, Mr. P. Woloson of Rodel and Dr. P. Pitner of SiBond.

References

1). Shibayama Kikai IntI, ltd., Tokyo, japan

2). Disco Corp, Tokyo, japan

3). Nissin Machine Works ltd., Hamamatsu, japan

4) .S. Matsui, "An experimental study on the Grinding of Silicon Wafers", Bull japan Society of Prec. Engr, vol 22, No 4, Dec '88

5). K. Puttick, "Energy Scaling Brittle-Ductile Transistions in Machining", Proc. of the Spring Topical Meeting for the American Society of Precision Engineering, p 14, Tucson, '93

6). L.j. Palkuti, P. Ling, P. leonov, H. Hawayoshi, R. Ormond and j. Yuan, "Radiation Response of CMOS/SOI Devices formed by Wafer Bond and Etchback", IEEE Trans. Nuclear Science, vol. 35, No 6, Dec '88.

7). Fa. Kugler, Salem, Germany

8). T. Abe, Y. Nakazato, M. .Daito, A. Kanai, M. Miyashita, "The Ductile Mode Grinding Technology Applied to Silicon Wafering Process", Proc. of the 7th International Symposium on Silicon Materials Science and Technology, p 207, San Francisco, '94.

9). M. Kerstan, H. lundt, A Huber, P .0. Hahn, M. Brohl, "Surface and Subsurface characteristics of ultraprecision ground silicon wafers", Proc. of the 7th International Symposium on Silicon Materials Science and Technology, p 218, San Francisco, '94.

10). ADE Corp., Newton, MA, USA

11). A Stephens, "Technique for Measuring the Depth and Distribution of Damage in Silicon Slices", Spring Meeting ECS, Boston, '86, p333.

12). H. lundt, M. Kerstan, R. Weiss, "Sub-Surface Damage Characterization of Silicon Wafers Using Scanning Infrared Depolarization (SIRD)", Proc. of the Spring Topical Meeting of the American Society of Precision Engineering, p42, Tucson, '93

13). T. Abe, A. Uchiyama, Y. Nakazato, "Wafer Thinning Without an Etch stop Down to 0.1um", Proc. of the First International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, vol 92-7, ECS, '91

14). GNM, Munich, Germany

15). IPEC Westech, Phoenix, Az, USA

16). R. Howard Strasbaugh Inc., San luis Obispo, CA, USA

17). Cybeq Systems, Menlo Park, CA, USA

18).Speedfam, Chicago, ll, USA

19).Presi, Grenoble, France

20).Discussion with K. lid a, Shibayama Kikai IntI. ltd., Tokyo, japan.

21).A. Yamada, B.l. jiang, G.A. Rozgonyi, H. Shirotori, 0. Okabayashi, M. Kawashima, "Structural Evaluation of Silicon-on-insulator Fabricated by a Direct Wafer Bonding and Numerically Controlled Polishing Technique", j. ECS, vo1138, No 8, August '91.

22).T. Matsushita, H. Satoh, M. Shimanoe, A Nieda, A Ogasawara, M. Yamagishi, A Yagi, "High Quality Thin Film SOl Technology using Wafer Bonding and Selective Polishing for VLSl's", 4 7th Annual Device Research Conf., IEEE, Cambridge, MA, june 1989, pp VB-1.

23).A Yamada, 0. Okabayashi, T. Nakamura, E. Kanda, M. Kamashima, 5th International Workshop on Future Electron Devices -3D Integration, Miyagi-Zao, May-june (1988), pp201.

24).J. Haisma, G.AC.M. Spierings, U.K.P. Biermann, j.A Pals, "Silicon-on-Insulator Wafer Bonding-Wafer 1bjnnjng Technological Evaluation", jjAP, vol 28, No 8, August 1989, pp 1426-1443.

25).G. Shahidi, B. Davari, Y. Taur, j. Warnock, M.A Wordeman, P. McFarland, S. Mader, M. Rodriguez, R. Assenza, G. Bronner, B. Ginsberg, T. ill, M. Polcari, T .H. Ning, "Fabrication of CMOS on Ultrathin SOl Obtained by Epitaxial

Lateral Overgrowth and Chemical-Mechanical Polishing", IEDM, 1990, pp 587-590.

26).T. Ohoka, T. Yoshitake, H. Kikuchi, K. Okonogi, "A Wafer Bonded SOl Structure for Intelligent Power IC", IEEE 5th International Symposium on Power Semiconductor Devices and IC's, (1993), ppI19-123.

27).Y. Hayashi, S. Takahasi, "Nitride-Masked Polishing (NMP) Technique for Surface Planarization of Interlayer-Dielectric Films", jpn j Appl Phs vol 32, 1993, pp 1060-1063

28).B. Neureither, C. Basa, T. Sandwick, K. Blumenstock, "Boron Nitride and Silicon Boron Nitride Film and Polish Characterization", j ECS, vo1140,no 12, 1993

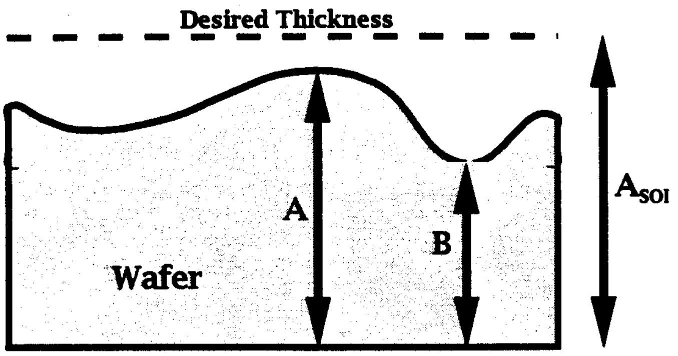
29).Y. Arimoto, H. Horie, N. Higaki, M. Kojima, F. Sugimoto, T. Ito, "Advanced Metal Oxide Semiconductor and Bipolar Devices on Bonded Silicon on Insulators", j. ECS, vo1140, No 4, April '93, ppI138-1143.

30).M. Hashimoto, A. Ogasawara, M. Shimanoe, A. Nieda, H. Satoh, A. Yagi & T. Matsushita, "Low Leakage SOl MOSFET's Fabricated using a Wafer Bonding Method", 21st Conference on Solid State Devices and Materials, Tokyo, japan, 1989, pp89-92.

31).T. Tanaka, H. Horie, S. Ando &5. Hijiya, "Analysis of P+ Poly Si Double-Gate Thin-Film SOl MOSFETS", IEDM, 1991, pp683-686.

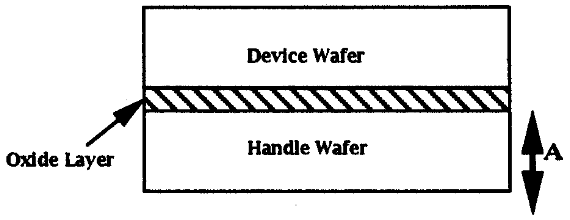
32).Won-Gu Kang, jong-Sun Lyu, Sang-Won Kang, Kwyro Lee, "Grounded Body SOl (GBSOI) nMOSFET by Wafer Bonding", IEEE EDL, vo116, No 1, jan '95.

33).M. Hashimoto, N. Nagashima, Y. Miyazawa, M. Shimanoe, H. Satoh, T. Matsushita, "Small Geometry SOl CMOS Cell Technology for High Density SRAMs", IEDM, 1991, pp 973-975.

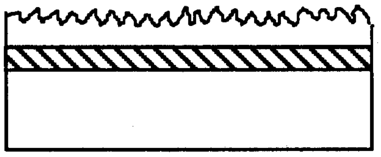


Bulk TTV = A - B
SOI TTV = A_{SOI} - B

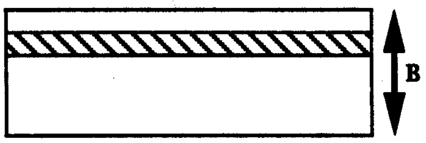
Fig 1 Bulk vs SOI TTV



Bonded Wafers



Grind Back



Polish to Final Thickness

SOI Thickness = A - B

Fig 2 Absolute Thickness Control

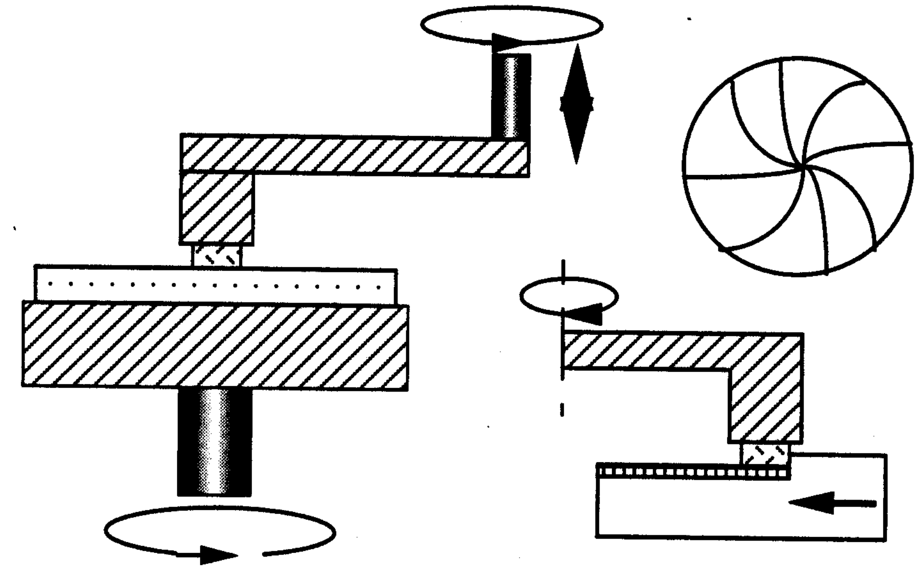


Fig 3 In-Feed Grinder

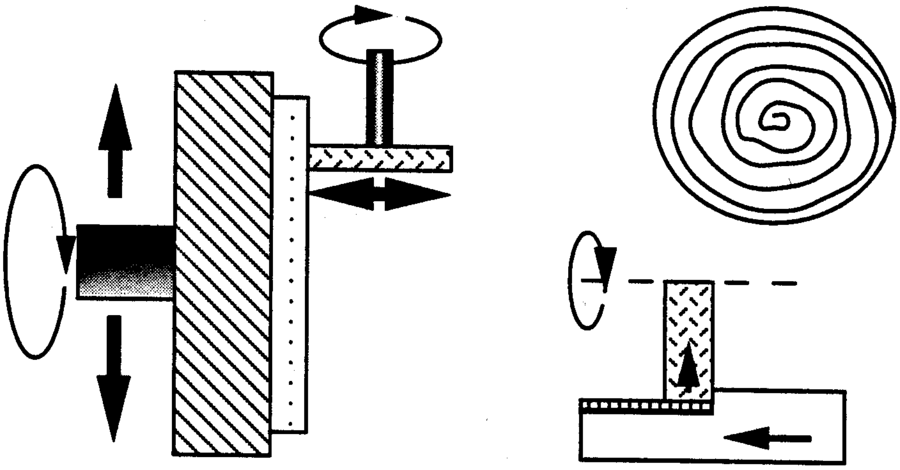
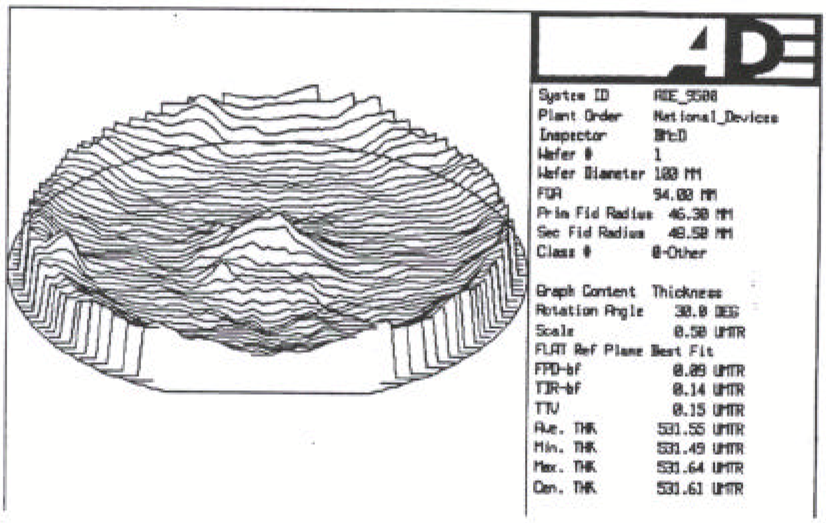


Fig 4 Horizontal Type Ultraprecision Grinder



```
System ID          ADE_9500
Plant Order        National_Devices
Inspector          BMcD
Wafer #            1
Wafer Diameter     100 MM
FQA                94.00 MM
Prim Fid Radius     46.30 MM
Sec Fid Radius      48.50 MM
Class #            0-Other

Graph Content      Thickness
Rotation Angle        30.0 DEG
Scale                 0.50 UMTR
FLAT Ref Plane Best Fit
FPD-bf                0.09 UMTR
TIR-bf                0.14 UMTR
TTV                   0.15 UMTR
Ave. THK            531.55 UMTR
Min. THK            531.49 UMTR
Max. THK            531.64 UMTR
Cen. THK            531.61 UMTR
```

Fig 5 +/-75 nm by In-Feed Grinding

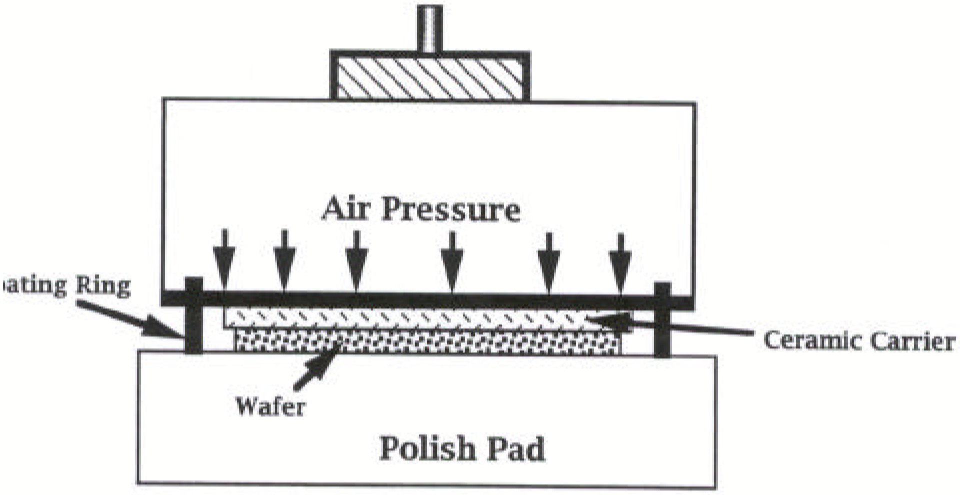
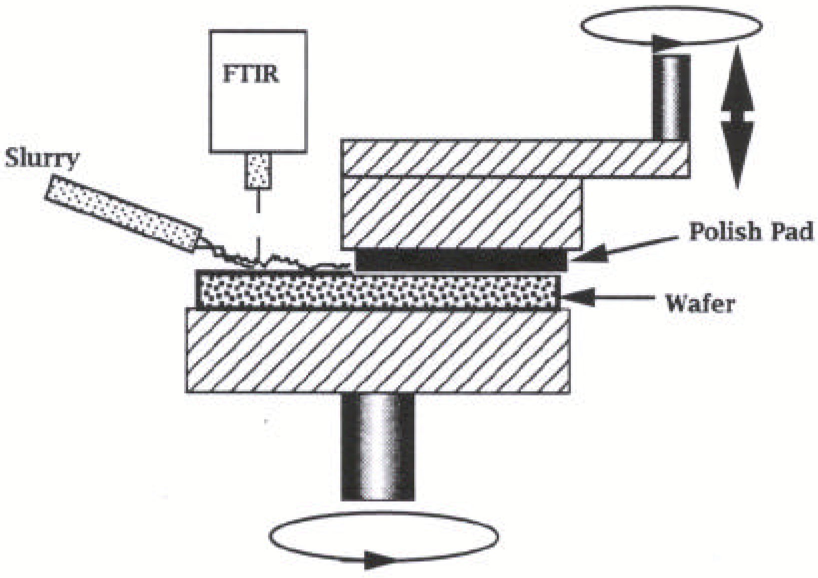
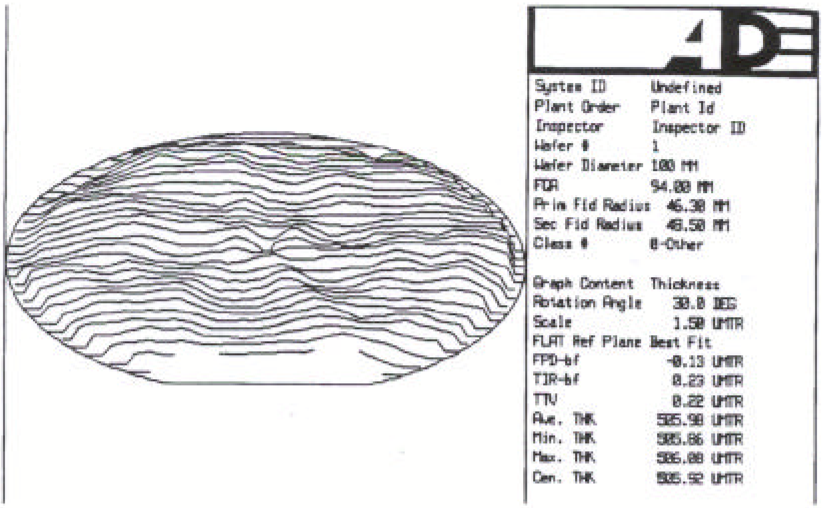


Fig 6 Cybeq Isoplanar 7000 Chuck



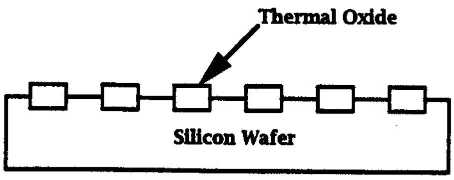
Configuration



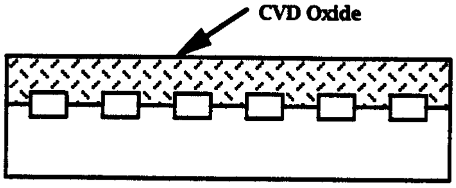
```
System ID         Undefined
Plant Order       Plant Id
Inspector         Inspector ID
Wafer #           1
Wafer Diameter 100 MM
FQA               94.00 MM
Prim Fid Radius   46.30 MM
Sec Fid Radius    48.50 MM
Class #           0-Other

Graph Content   Thickness
Rotation Angle      30.0 DEG
Scale               1.50 UMTR
FLAT Ref Plane Best Fit
FPD-bf             -0.13 UMTR
TIR-bf              0.23 UMTR
TTV                 0.22 UMTR
Ave. THK          505.98 UMTR
Min. THK          505.86 UMTR
Max. THK          506.00 UMTR
Cen. THK          505.92 UMTR
```

+/-110nm Thickness Control

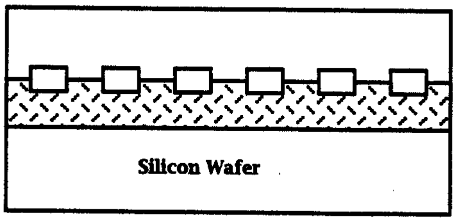
Fig 7 In-Feed Polisher



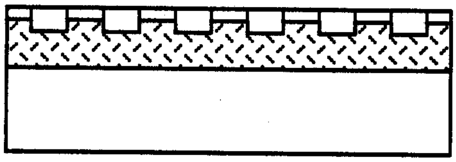
Local Oxidation



Oxide Deposition And Smoothing



Wafer Bonding



Selective Polish

Fig 8 Polish Stop

Mechanical Thinning SOI Development

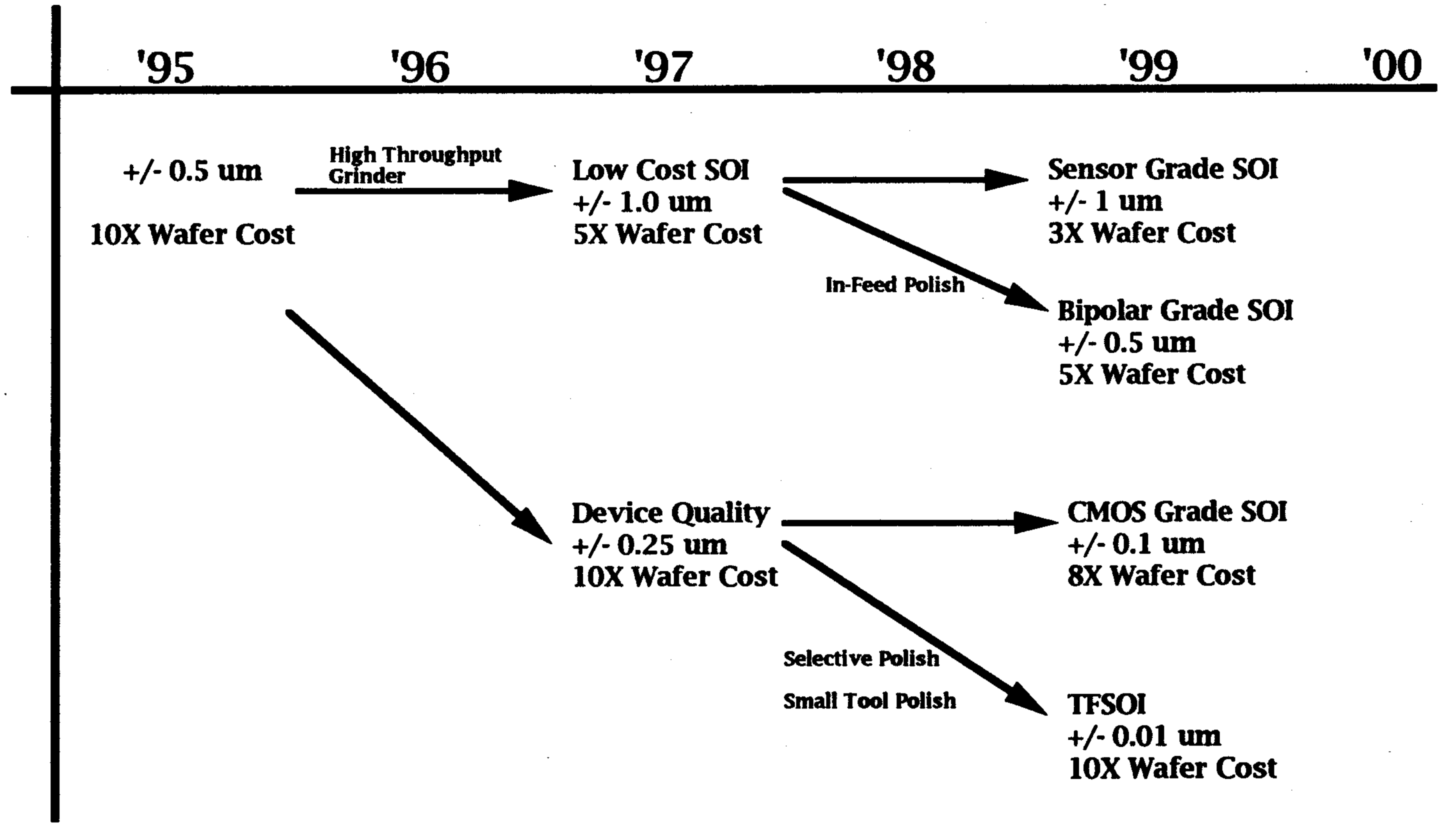


Fig 9