

Single crystal micromachining using multiple fusion bonded layers

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ABSTRACT

Multi-layer structures have been fabricated using Fusion bonding. The paper shows void free layers of between 2 and 100 microns that have been bonded to form multi-layer structures. Silicon layers have been bonded both with and without interfacial oxide layers.

Bonded layers have been shown to be void free by InfraRed transmission and by Scanning Acoustic Microscopy. The silicon layers and the interfacial oxide layers have been patterned before bonding to produce novel micromachined structures with pre-etched cavities. Silicon layers have been bonded after patterned implantation to form buried interconnects.

These multi-layer structures are an extension of SOI MEMS and maintain the advantages of this technology while extending the possible applications. The paper shows released single crystal silicon structures with buried cavities, manufactured using fusion bonding of pre-patterned layers. Silicon layers can be used as precise spacer layers for microphotonic and other devices.

Processes have been developed to enable patterned and implanted layers to be bonded and thinned reliably and with good yields. Structures can therefore be made of single crystal silicon as an alternative to the polysilicon structures from typical surface micromachining processes. Lower stress and more uniform layers are two of the potential benefits of this technique

Keywords: SOI, MEMS, Fusion bonding, Direct wafer bonding, Multi-layer substrate, DRIE, Buried cavities, MOEMS

1. INTRODUCTION

Fusion bonding to produce multiple layer structures is an extension of the growing field of SOI MEMS. MEMS based on Silicon on Insulator wafers (SOI MEMS) has been well documented.^{1,2,3,4} SOI MEMS has become an important technique because it allows single crystal silicon to be used to make microsystems.

SOI and fusion bonding of silicon wafers has been used to manufacture a variety of MEMS products. Accelerometers⁵ and pressure sensors⁶ have been demonstrated. Optical microsystems (MOEMS) benefit in particular from the SOI approach and it is possible to fabricate waveguides, mirrors and optical switches using SOI MEMS.^{2,3}

Single crystal silicon has a number of advantages over polysilicon for microsystems manufacture. The residual stress in the film is minimal² mechanical and electronic properties are superior to polysilicon⁷ single crystal structures can be made flatter and smoother than polysilicon⁸ and single crystal layers are not limited to a few microns in thickness⁷. There are limitations to the use of SOI for microsystems however. It is difficult to obtain commercial SOI with varying specifications, the buried oxide (BOX) in particular is often less than 1 micron. Even custom SOI manufacturers are limited to 3 microns BOX thickness.

A second difficulty is that it is hard to fabricate distributed electrodes under micromechanical components.² In addition, it is often necessary to perform photo and metallisation processes after release of the silicon structure. This can lead to complicated process flows.

The use of multiple fusion bonded layers addresses some of the limitations of SOI MEMS. Gui et. al. demonstrated a multi-layer substrate (MLS) that enables thicker sacrificial layers to be used than with the conventional SOI approach. The manufacture of this multi-layer substrate was demonstrated with a polysilicon layer sandwiched between two single crystal layers with or without a silicon dioxide layer in between.⁹ (Figure 1)

In this paper it is shown that similar structures can be made with a single crystal silicon intermediate layer, and indeed with more than three silicon layers. These layers can be formed with or without an intermediate silicon dioxide layer. A novel technique is shown that enables patterned layers to be bonded producing a pre-aligned buried mask layer for DRIE etching. This process is discussed in more detail by Gormley et. al.¹⁰

By using a sacrificial wafer bonding technique, very uniform silicon layers can be formed as any of the layers in a multi-layer structure, using standard SOI manufacturing techniques.^{11,14}

Bonding can be performed over pre-etched cavities to produce a suspended membrane. It is also possible to use DRIE etching to etch a cavity through the handle wafer to release suspended microstructures.

2. FABRICATION PROCESS

2.1 SOI Manufacture

SOI manufacture by wafer bonding and mechanical thinning is the technique that has been used to manufacture these structures. The bonding of silicon wafers is well documented and is not discussed in detail here.¹² Using precision grinding it is possible to produce handle wafers with a total thickness variation (TTV) of 0.5 μm . After CMP to prepare the surface for bonding the TTV can be kept below 1 micron. This ultra -flat handle wafer is then used as the reference plane for thinning the SOI layer after bonding. As can be seen from figure 2, the SOI layer should be manufacturable to better than +/- 1 μm . In reality, with control of the shape of the wafer after grind, the SOI tolerance can be controlled to better than +/- 0.5 μm . See figure 2.¹³

The wafer bonding process is normally performed with a thermal oxide layer of between 0.4 and 3 μm formed on one or both of the wafers. It is possible to bond wafers without this oxide layer, and this has been done with both hydrophilic and hydrophobic surfaces.¹⁵

After direct wafer bonding the wafers are annealed at a temperature above 1000°C to complete the fusion bond. All SOI was manufactured under standard manufacturing conditions at BCO Technologies.

2.2 Multiple layer bonding

After the manufacture of SOI wafers, a third layer is bonded to the SOI to form a multi-layer substrate. Wafers have been bonded both to the device side of the SOI wafer and to the handle side. The bonding process used standard SOI bonding processes and equipment and can be done with a similar high yield to that achieved in standard SOI processing. A thermal oxide is normally used on one or both of the wafers, but the wafers can be bonded without this oxide or with LPCVD oxide. An IR image of a void free bond is shown in figure 3.

Once the third layer is bonded it is thinned using precision grinding. The uniformity of this third layer will not be as good as the first layer, because the control of the wafer shape is not as precise. Each subsequent layer will be less uniform than the previous layer. While the thickness of the first SOI layer can be controlled to +/- 0.5 μm by this method, the second SOI layer will have thickness uniformity of +/- 0.7 μm . Third and subsequent layers will have uniformities of +/- 1 μm or more.

In order to minimise the non-uniformity of the silicon layer, a sacrificial wafer method can be used. In this method, as SOI wafer is prepared with the SOI layer controlled to the required thickness. The sacrificial wafer approach can be used with SOI from other sources, enabling much thinner films to be bonded than are possible with mechanical thinning. The SOI layer of this wafer is then bonded to the structure and the handle wafer is removed. The BOX in the sacrificial wafer acts as a stop for a wet etch or CMP process. Using this method it is possible to fabricate layers with both precise control of thickness and low TTV. The sacrificial wafer bonding is discussed in detail by Spiering et. al.¹¹ and S. d'Aragona et.al.¹⁴

2.3 Bonding of patterned layers

By DRIE etching of either the substrate or one of the bonded silicon layers, cavities are formed on the surface of the wafer. These are printed using a double sided mask aligner with alignment targets placed on the back of the handle wafer. A subsequent layer is then bonded over these cavities and thinned back to the required thickness.

One problem associated with bonding over cavities is caused by the CMP process that is used to polish the wafer surface. Depending on the size of the cavity and the thickness of the silicon layer, the silicon will deform into the cavity during the CMP process. When the CMP is finished, the silicon is then thicker over the cavity than it is on the rest of the wafer. See figure 4.

To avoid this, the sacrificial wafer technique is again used. The SOI layer is transferred to the pre-cavitated wafer and then the handle wafer is removed by a combination of precision grinding and either CMP, wet etching or DRIE etching, using the oxide layer as a stop layer.

When bonding over pre-etched cavities it has been reported by S. d'Aragona et. al. that the deflection of the cavities after thinning is shown to vary according to the bonding ambient, the presence of oxide layers and the thermal treatment that the wafers have undergone after bonding.¹⁴

Their results showed that for a single anneal at 1000°C, the wafers joined in air were convex in shape.(ref) This fits with the results seen on the 5 µm thick membranes bonded in this test where the majority of the membranes were convex in shape. The displacement of the membranes at the edge of the wafer was higher than the displacement at the centre, indeed, many membranes at the centre of the wafer showed a negative displacement, or concave shape. The displacements were measured on a Tencor Alpha Step. Micrographs of membranes are shown in figure 6. The displacement of the centre of the 5µm thick membranes are plotted against the membrane diameter in figure 5. A summary of the membrane deflections is shown in table 1 below.

Membrane diameter (µm)	5 micron thick membrane deformation in nm, +ve is convex in shape		19 micron thick membrane deformation in nm, -ve is concave in shape
	Centre of Wafer	Edge of Wafer	Centre of Wafer
200		+1200	
400	-75	+2500	
600			+100
800	-205	+14000	
1000		+12000	+300

Table 1: Summary of membrane deflection for 5µm and 19µm membranes

19 µm membranes that were formed in the same way showed little deflection. A 1000 µm diameter membrane showed a maximum deflection of 300 nm and a 600 µm diameter membrane showed a maximum deflection of 100 nm. Both these were convex in shape. Figure 7 shows SEM micrographs of 19 µm thick membranes bonded over 3 µm cavities and thinned using the sacrificial wafer method. Further investigations are planned to determine whether or not the 5 µm membranes have undergone plastic deformation due to slip, and to determine the processing limits for this.

2.4 Patterning and releasing layers

DRIE etching is used to either pattern the membrane structures, or to release the membrane structures by DRIE etching the handle wafer. Deep etching is performed using a modified Bosch process as discussed by Gormley et al.¹⁰. If there is an oxide layer on the membrane structure, this can be removed by HF releasing and drying. DRIE etching of all these tests were performed under manufacturing conditions at BCO Technologies.

3. FORMATION OF BURIED MASKING LAYERS BY WAFER BONDING

A novel process has been developed to enable the manufacture of a buried masking layer. A standard SOI wafer is manufactured, with the SOI layer being made to the required specification for the active layer. An oxide layer is either grown or deposited on this SOI layer. This oxide layer is patterned by double sided photolithography, using alignment marks on the back of the handle wafer and RIE oxide etching. After stripping the resist, a third wafer is bonded to this patterned oxide and thinned to the required specification. This layer can be patterned by photolithography and etched using a DRIE silicon etch. This etch will open a hole in the top layer and etch down to the buried oxide between the top layer and the middle layer in the stack.

Where the oxide has been etched in the previous patterning step, the silicon will continue to be etched until the etch reaches the second buried oxide layer. This process produced an active layer that is not planar with the top surface of the wafer but is separated from the top surface by the thickness of the top silicon layer. Figure 8 shows a schematic description of the process. Figure 9 shows a structure that has been fabricated using this technique. This novel process is enabled by a well controlled, flexible and robust DRIE process at BCO Technologies' MEMS manufacturing facility.

4. SUMMARY

Multi-layer silicon on insulator wafers have been manufactured using standard SOI manufacturing methods under well controlled and robust processes at BCO Technologies' MEMS manufacturing facility. Two and three layers of silicon have been bonded on a silicon substrate and each of those layers have been thinned to an accuracy of better than +/- 1 µm. Silicon layers have been bonded using a sacrificial wafer technique that enables highly uniform layers to be formed.

Layers have been bonded over pre-etched cavities. For layers of 5 µm or less this has produced deformation of the silicon layer over the cavity. The reasons for this are under further investigation. For thicker layers over cavities there is no appreciable deformation of the membranes formed.

A novel technique has been demonstrated that enables a buried mask layer to be formed by patterning before bonding. This buried masking layer is then used to pattern both the top layer and an underlying layer at the same time.

Multi-layer structures such as those demonstrated can address some of the limitations of SOI MEMS. Silicon layers can be used as sacrificial layers and increase the depth of cavities that can be formed beneath single crystal structures. (2 refs) With further developments it may be possible to use a layer in a multi-layer substrate to form electrodes distributed under components in a subsequent layer.

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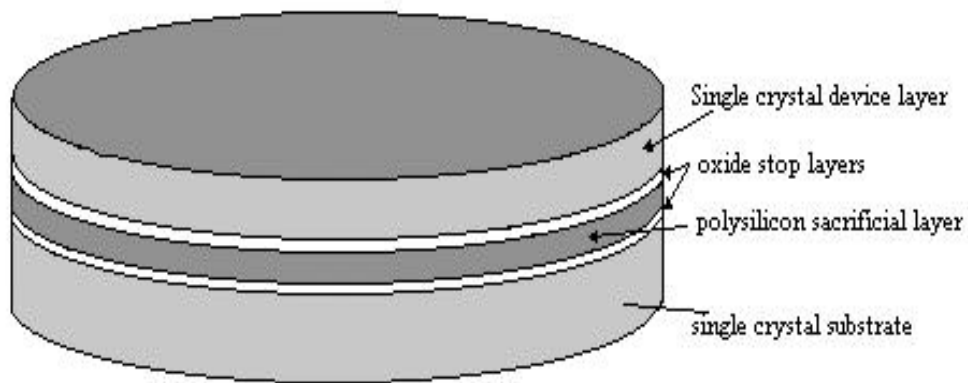


Figure 1: Multi-layer substrate as described by Gui et. al. ⁹

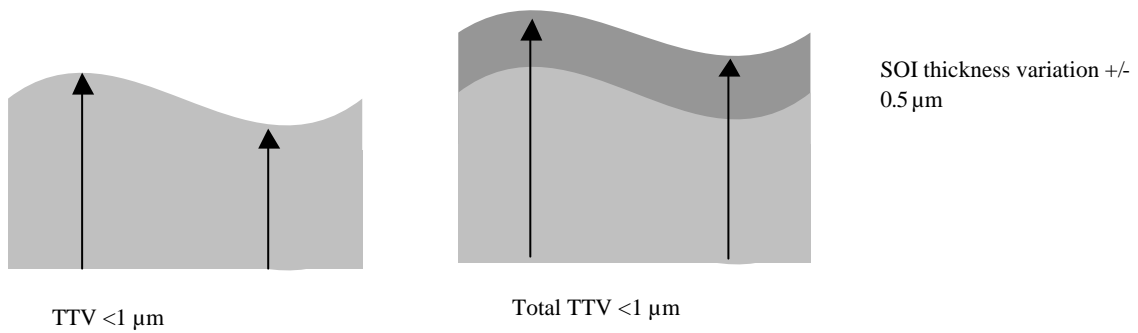


Figure 2: Precision ground handle and SOI

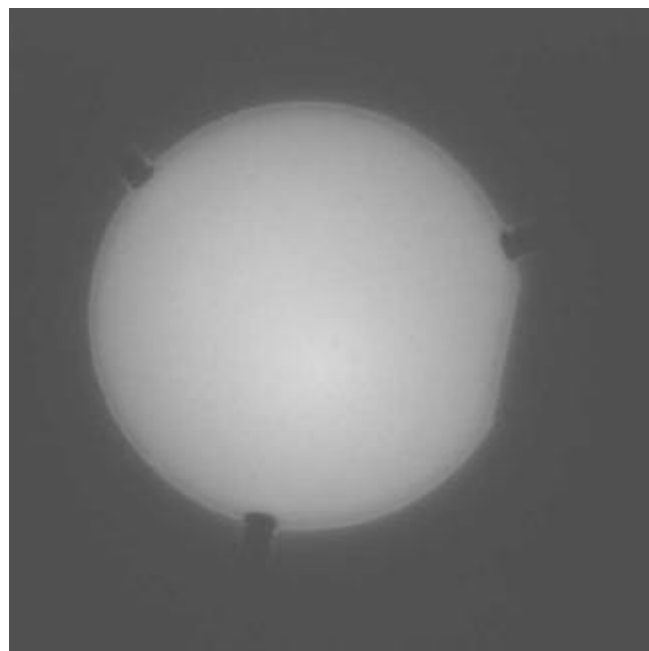


Figure 3: IR image of void free bond

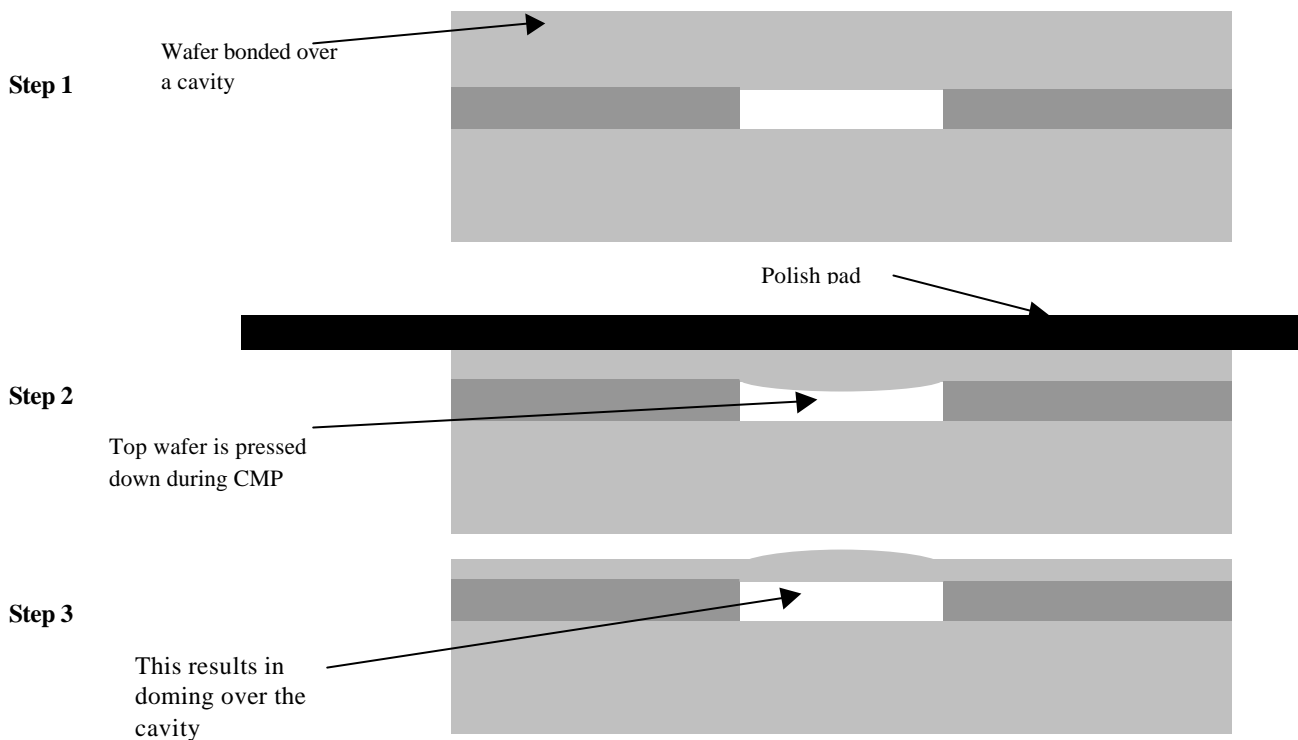


Figure 4: Effect of CMP over cavities without a polish stop layer

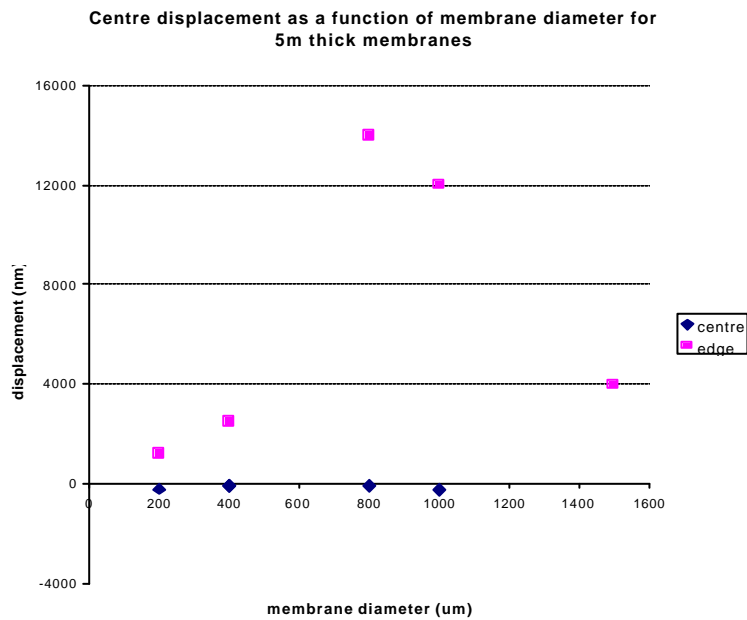
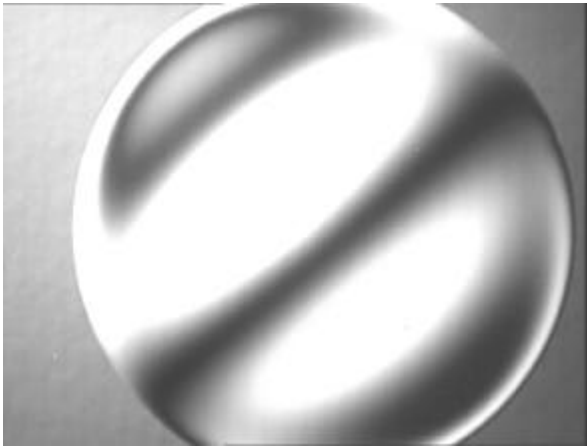
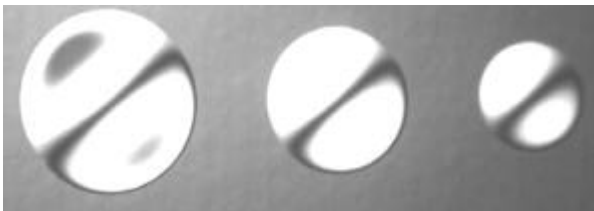


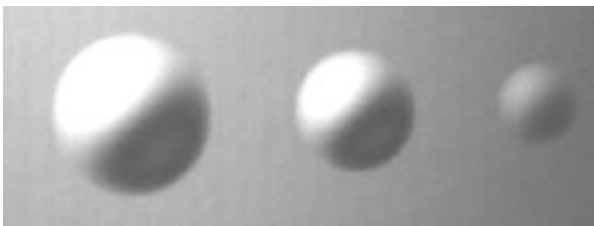
Figure 5: Comparison of 5 μ m thick membranes at the centre and edge of the wafer



5 μm thick membrane. Diameter is 2000 μm .
Membrane is convex and at the wafer edge



400 μm , 300 μm and 200 μm diameter membranes of 5 μm thick silicon. These membranes are convex and are at the wafer edge



Similar membranes to above, but at 1/2 radius. These wafers show less displacement and are convex in shape



600 μm and 400 μm membranes at the centre of the wafer. These membranes are concave

Figure 6: Micrographs of circular membranes showing curvature in relation to position on the wafer

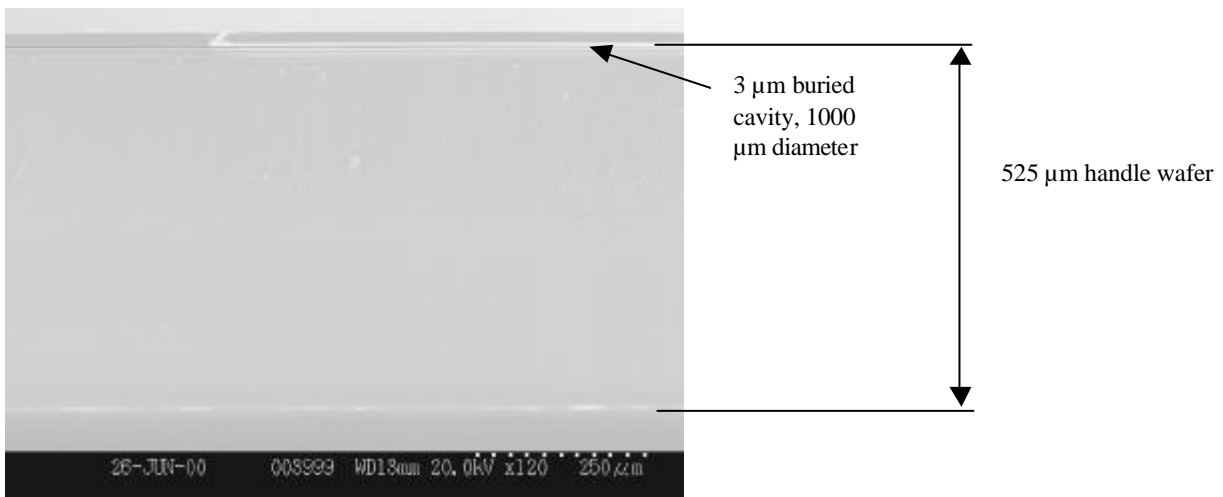
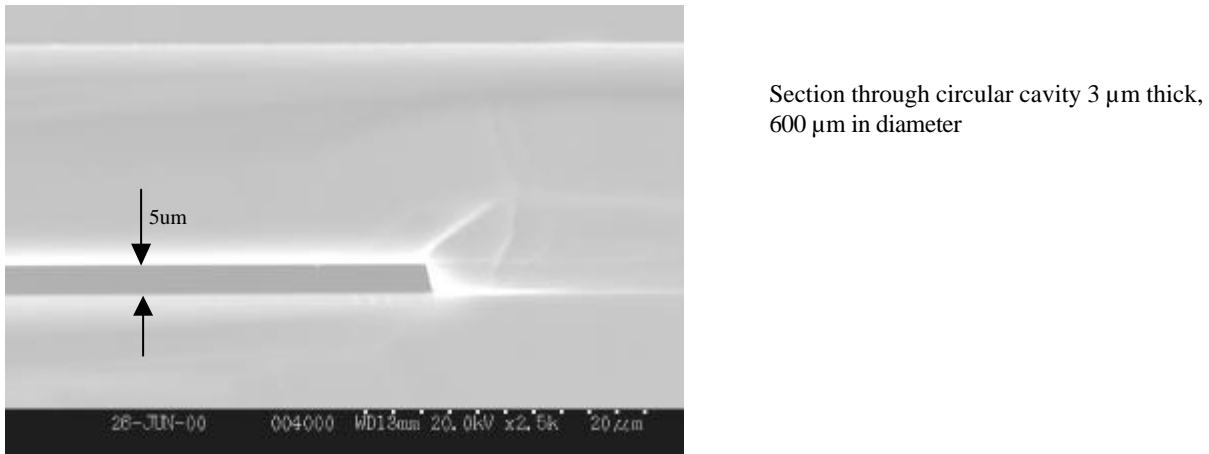
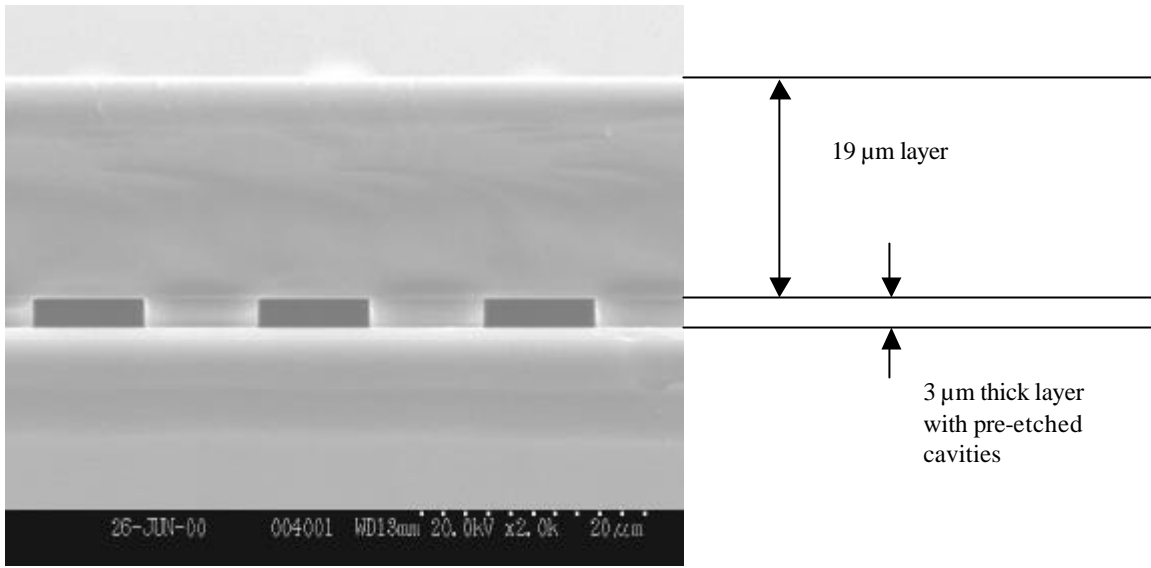


Figure 7: Scanning electron micrographs of bonding over cavities

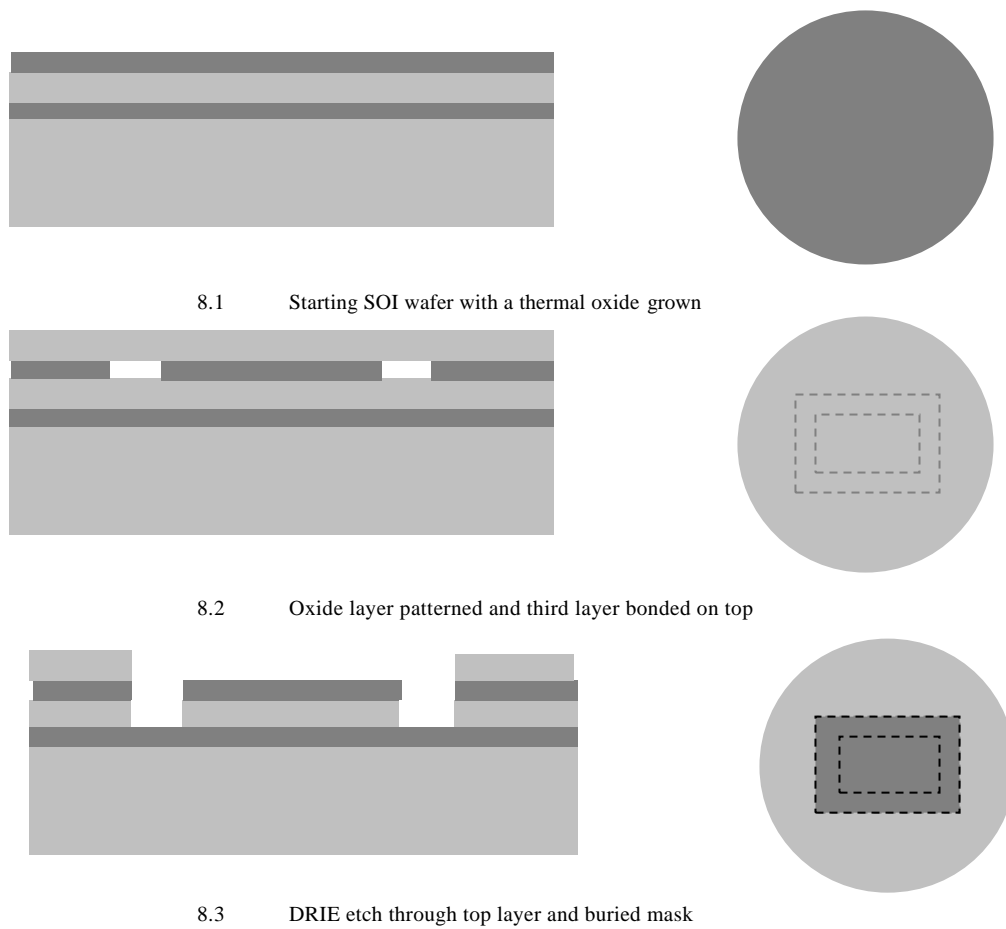


Figure 8: Schematic of buried masking process

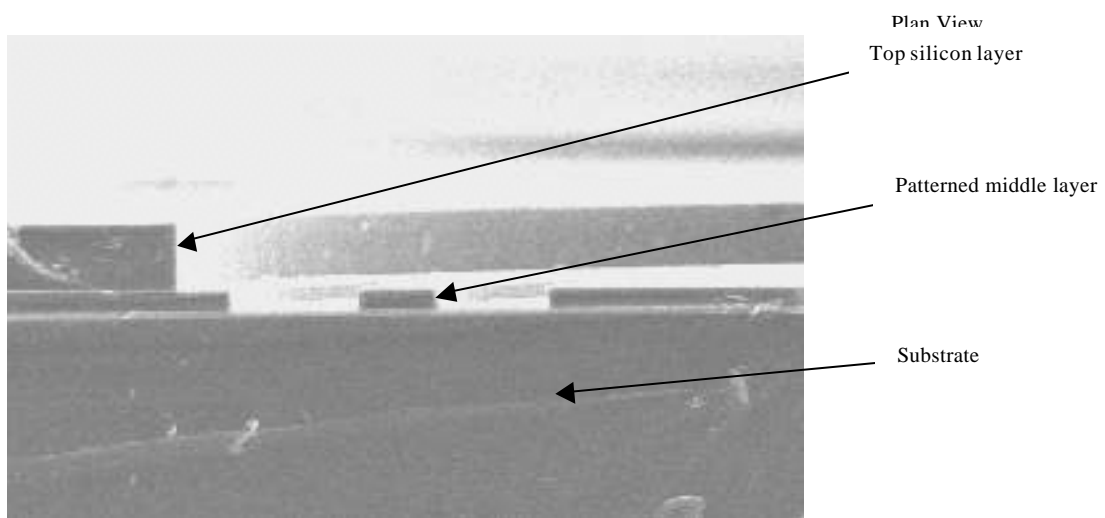


Figure 9: SEM micrograph of structure formed using wafer bonding with a buried mask layer