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A FULLY OXIDE-ISOLATED BIPOLAR TRANSISTOR INTEGRATED CIRCUIT PROCESS.

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ABSTRACT

Bonded wafer SOI provides an attractive solution for bipolar technology. Transistor quality can be as good as the bulk silicon technology while collector substrate capacitance can be reduced by at least an order of magnitude by the combination of the buried oxide and dielectric filled trenches. In order to gain the full benefit of SOI however, it has been necessary to develop a process which offers good yield for the combination of trench isolation on SOI. Practical results on R.F. circuits in the 500MHz to 2 GHz communications bands are shown.

OBJECTIVE

It is known that the combination of trench and SOI can lead to the generation of stress induced defects. In this programme of work, experiments were performed to investigate and minimise the effect of trench processing on defect generation as observed by Secco etching of cleaved samples. Active area to trench spacing was investigated to eliminate the observed defects while minimising added process complexity .

APPROACH

Bonded wafer SOI was used as the starting material for a lOps transit time single layer polysilicon bipolar process with 0.75um feature size (1). Conventional collector and epitaxy technology was used in the construction of the NPN transistors prior to trench formation. Trenches were formed by reactive ion etching (RIE) down through the epitaxy and bonded silicon, taking care to minimise etching of the buried oxide. The trench was first thermally oxidised to a thickness of 1000 A, and then filled with polysilicon. A nitride mask was used to define active areas and prevent field oxidation of the collector and emitter/base regions.

Two types of devices were then fabricated:-

.Test structures with P- base active area region only and trench .

.Complete NPN device with collector, base, emitter and trench.

For the test structures with the simple active~area then the nitride mask was enclosed by
trench at three different separations: 0.75um (A); O.50um (B); and 0.25um (C) as drawn in figure 2. There was a fourth structure in which the trench and nitride overlapped by O.25um (D) and one in which the nitride mask was taken right across the top of the trench and outside by 0.75um (E).

Oxidation of the field areas outside of the nitride mask, including unmasked trench, was then carried out as represented in figure 3.

The idealised cross-section of a NPN transistor fabricated with the bonded SOI material is shown in figure 4.

A shallow N type emitter was formed by implanting N type into the polysilicon and thermally diffusing out dopant to form the NPN transistor. Metal contact was achieved by depositing a further layer of oxide and etching contacts followed by a metal deposition and patterning stage. Resistors were constructed using the poly silicon layer.

Minimum drawn dimensions were 0.75um for features such as the trench and emitter, and a metallisation pitch of 2.75um was imposed. Two layers of metal were used for the interconnection, separated by an oxide dielectric.

Initially, single polysilicon NPN devices (figure 4) were fabricated with an active area to nitride mask separation of 0.5um from the enclosing trench. This of course lead to defect generation, as discussed in the material results, but the small circuits used were found to be operational in some cases.

Completed samples were cleaved and Secco etched for 15 seconds to reveal defects in the cross-sections of bonded silicon crystal.

MATERIAL RESULTS

It was observed (figures 5,6) that where the nitride mask of the active areas was separated by 0.25um (A), 0.50um (B) or 0.75um (C) from the inner edge of the trench then stress induced defects were formed adjacent to the top corner of the trench. They were also observed in the centre of the active area as a long vertical line from the surface down to the buried oxide. Defects were also observed on the outer edge of the trench but these are

benign as devices are not fabricated in the epitaxial and the bonded silicon between two trenched regions. The stress has been induced by the oxidising "birds beak" extending down the trench wall between the polysilicon and the bonded silicon film.

In the case where the nitride mask intersected the trench by 0.25~m (D) then defects were not observed on the inner edge of the trench:(figure 6). It was also seen that the vertical ,- defect in the centre of the active area was not present- Defects were still seen adjacent to the outer edge of the trench in the region between devices.

In the last configuration, where the nitride mask was taken right across the top of the trench and outside by 0.75um (E) then defects were not observed on either side of the trench or in the centre of the active area (figure 6). However, this method with the simple trench fill did lead to recessing of the top of the trench and it is much less planar-

In each of the five styles (A) -(E), the care in minimising the etching of the buried oxide at the base of the trench appears (figure 5,6) to have prevented stress induced defects being created from the corners adjacent to the buried oxide.

In the case of a NPN device, with an active area nitride mask separated by 0.50um from the enclosing trench, defects are seen (figure 7) in different positions from the equivalent simple test structure (B). The stress induced defects are now effected by the presence of highly doped regions such as the deep collector and buried collector. The stress appears to be relieved at the left and right edges of these highly doped regions, resulting in damage to the epitaxial and bonded silicon film. This prevents a clear picture of the stress induced damage from being observed, as was the case of the simple test structures. The highly doped regions screen the source of the stress preventing a clear analysis to be made.

Devices were also fabricated using style D with the nitride mask intersecting the trench by 0.25um, The SEM cross section in figure 8 shows that the active device region is now largely clean of defects.

It can be seen that stress has induced defects in the region outside of the device trenches under the field oxide. This is a region where active devices are not formed and so presents no influence on device performance. An enlargement of the trench (figure 9), however, shows that there are still some random occurrences of stress induced defects in some transistors, albeit on a much reduced scale.

The knowledge that was gained from these examinations of cross-sections was then used to interpret the electrical results of fully fabricated devices.

Although the defects are a serious cause for concern, and revised structures are being investigated, some simple circuits were made on the same test mask, with results

confirming that SOI is advantageous both in low power operation and in improved bandwidth compared to their bulk silicon equivalents. (1)

TRANSISTOR RESULTS

Electrical evaluation of NPN devices fabricated with style B showed that occurrences collector-emitter leakage were common as demonstrated in the Gummel plot in figure 10. This along with all the Gummel plots was taken at a fixed V cb of 0V. It is clear that the collector -emitter leakage is a direct result of the stress induced defects in the epitaxy and bonded silicon film of the devices (figure 7).

With the modified trench (style D) which is intersected by the active area then the Gummel plot (figure 11) shows emitter -base leakage. This is indicative of some residual stress in the silicon in the emitter region and is caused by the proximity of the trench to the emitter. In this case, the trench was moved inwards to intersect the active area and so reducing the emitter to trench distance by 0.75I-1m.

Following on from this, transistors were analysed with the trench to emitter spacing increased whilst maintaining an intersect of active area and trench. A substantial improvement in emitter -base leakage was observed in the Gummel plot (figure 12). This transistor architecture would be appropriate for logic in low power circuit applications.

It has also been observed that NPN devices with a deep collector guard ring show no leakage (figure 13). This demonstrates, along with non-trench devices on both bulk silicon and bonded SOI, that the emitter -base architecture is sound when not disturbed by the stress from the trenches. For the Guarded devices, used on bulk silicon to reduce parasitic PNP action, it is thought that the heavily doped deep collector ring around the base area acts as a stress relief mechanism. Thus the Guarded devices show good potential for very low power analogue and as they should not contain the high parasitic capacitance that is normally experienced on bulk silicon.

Transistor parameters are shown in table 1. Of particular note is the low collector- substrate capacitance Cjs.

	Measured on First Test batch	Target Values
Emitter Area	0.75 X 1.25μm^2	
HFE	62	100
VAF	63 V	40 V
RB	840 ohms	550 ohms
RE	13.4 ohms	25 ohms
RC	296 ohms	175 ohms
TF	9.6 ps	10 ps
CJE	11.6 fF	6 fF
CJC	15.1 fF	15 fF
CJS	~ 4 fF	4 fF
BVCEO	5 V	5 V

Table 1. Measured and target SPICE parameters for a minimum geometry double base NPN transistor .

The measured figures, even on this first batch, were substantially in line with the targets, except for a rather low HFE. The transition frequency ~ FT, peaked at 11 GHz but subsequent improvements have improved the performance to give a peak FT of 13GHz and BV_{CEO} of >7V. However, it is emphasised that this is a research programme; final device characteristics are still to be optimised. These improved transistors were used for the amplifier results section.

AMPLIFIER RESULTS

A simple amplifier circuit, aimed at low power operation in the 500MHz -2GHz region was included on the test chip. The results are shown in figure 14 and give a gain of 18dB at 900MHz at a power of only 8m W .

The noise figure measurements are shown in figure 15. The noise figure at low frequency was measured to be less than 2.5dB, rising as expected with frequency. At the emerging communications frequencies of 900 MHz, as in the case of GSM, the noise is still less than 3 dB. This easily meets the specification for GSM which specifies that the noise needs to be less than 6 dB in the RF amplifier section. In addition, the noise figure is only slightly sensitive to the power consumption.

CONCLUSIONS

Systematic analysis of stress induced defects has been used to define a trench isolated SOI process for bipolar transistors. We have found that the optimum transistor style is circuit dependant and can be suited to low power logic or low power analogue.

Preliminary circuit results show excellent low power performance which easily meets the emerging 900MHz GSM communications specification.

Bonded SOI has clearly shown that it is compatible with traditional bipolar technology and its manufacture.

The benefits of a fully oxide isolated bipolar transistor integrated circuit process have been demonstrated and show a firm foundation for a whole new era in enhanced bipolar technology.

ACKNOWLEDGEMENTS

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[1] P. Saul, "The benefits of bonding silicon on insulator for bipolar ICs", IEE Review Nov. 1994, pp 263-266.

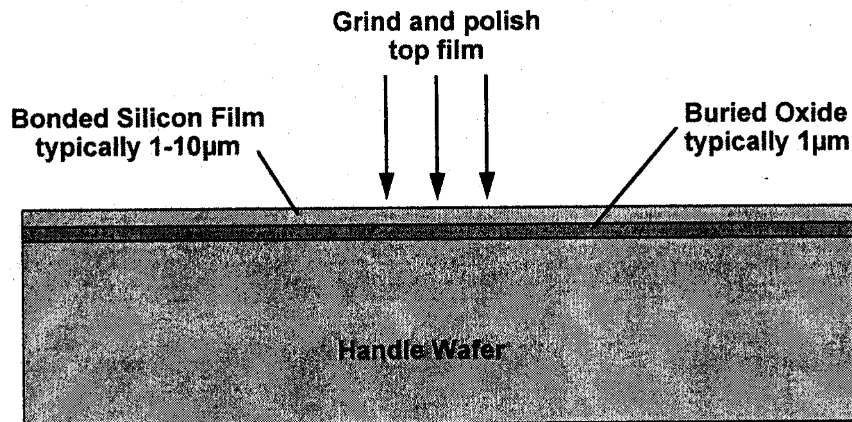


Figure 1. Bonded wafer structure.

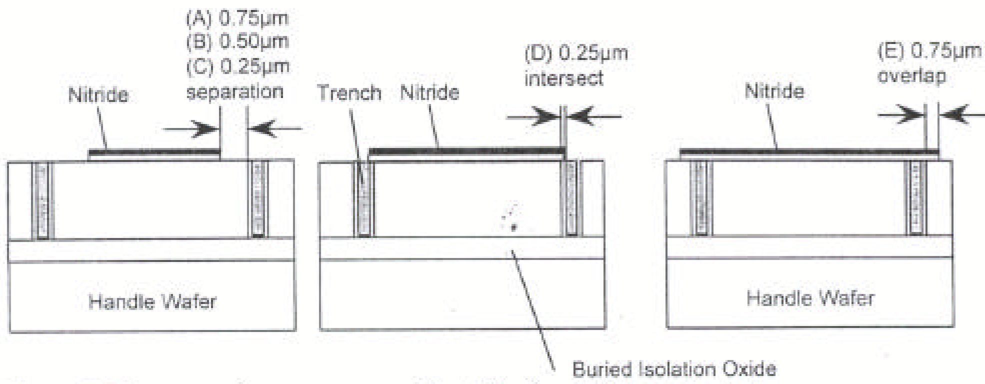


Figure 2. Diagram of test structures (A) - (E) after nitride mask etch.

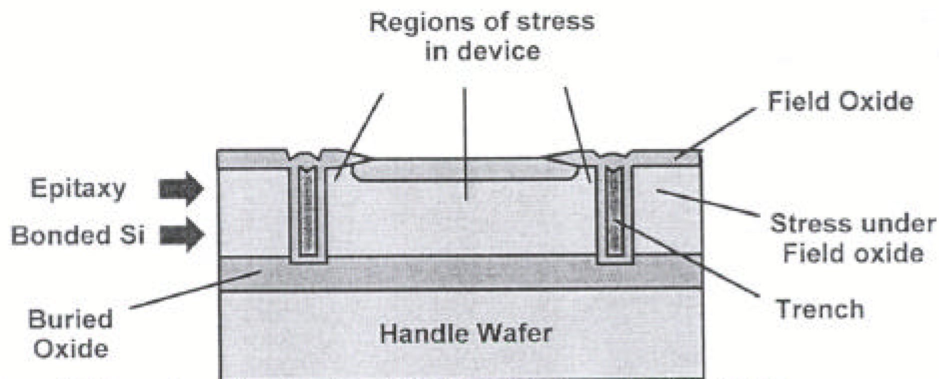


Figure 3. Schematic of test structure (B) after oxidation of the field areas.

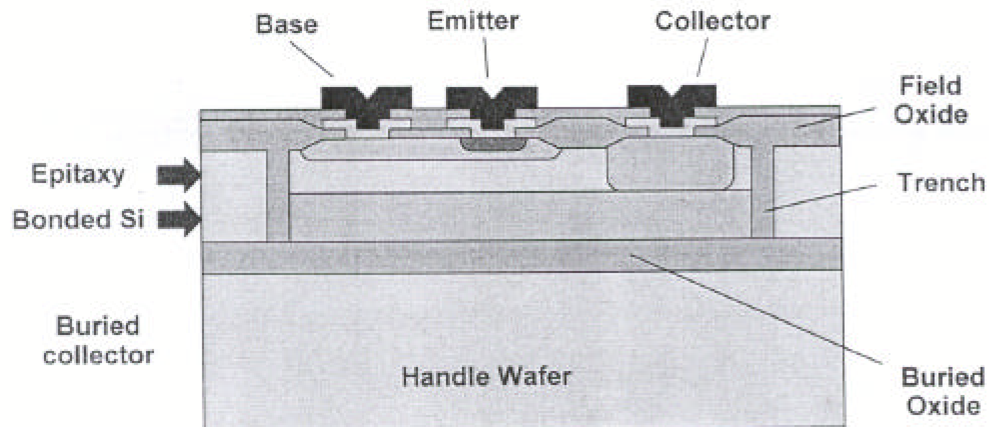


Figure 4. Cross section of an NPN transistor in bonded SOI.

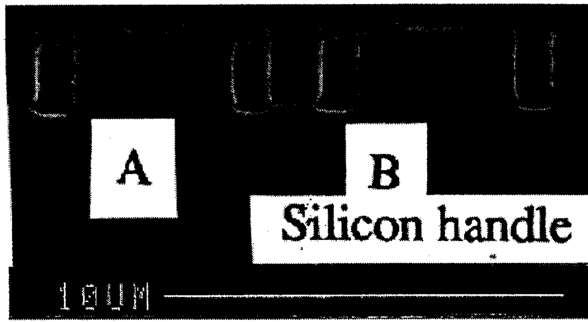


Figure 5. SEM photo of Secco etched test structures A and B.

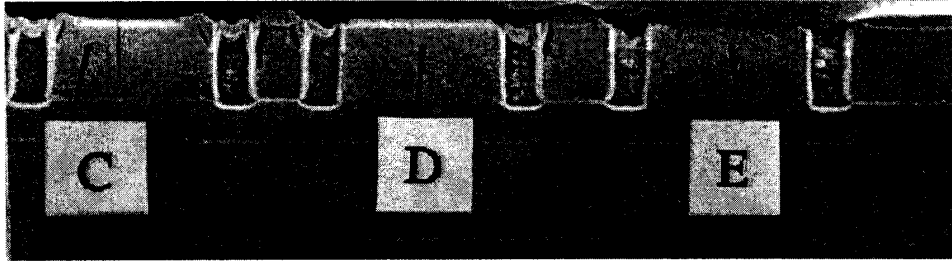


Figure 6. SEM photo of Secco etched test structures C, D and E.

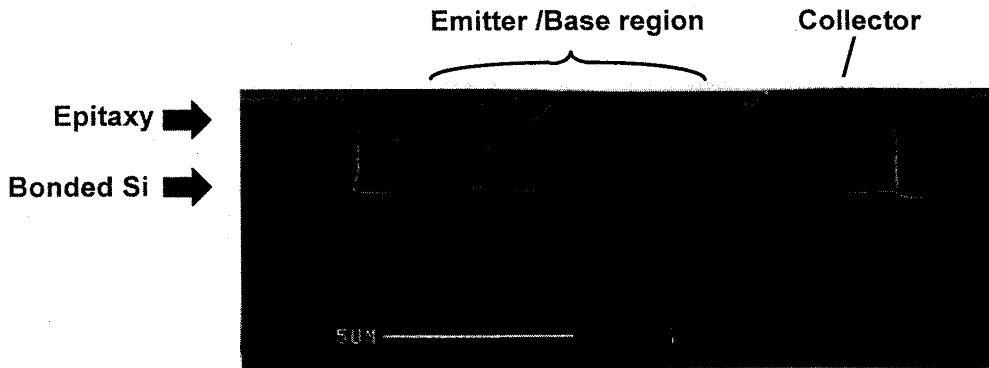


Figure 7. SEM photo of Secco etched NPN transistor with original trench (style B).

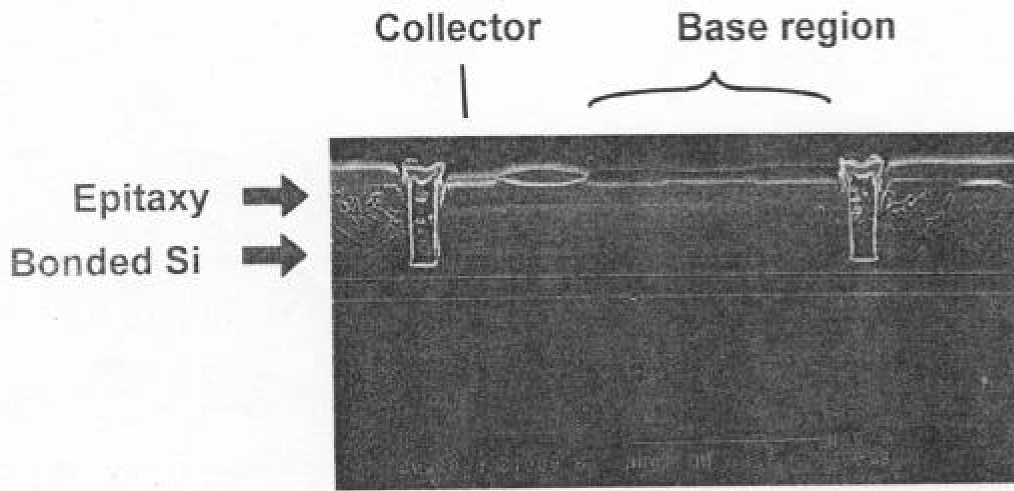


Figure 8. SEM photo of Secco etched NPN transistor with modified trench (style D).

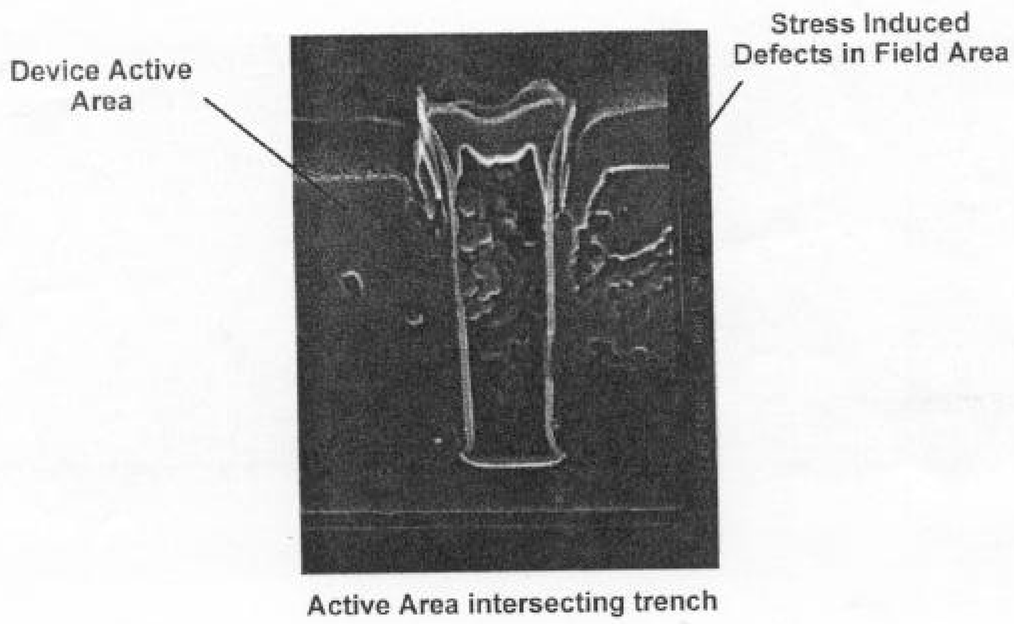


Figure 9. Enlargement of modified trench (style D) after Secco etch.

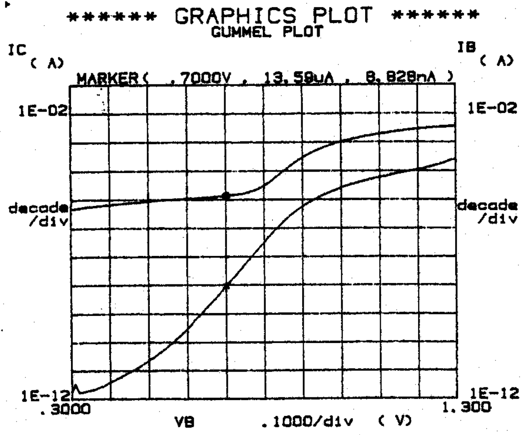


Figure 10. Gummel plot of NPN transistor with original trench.

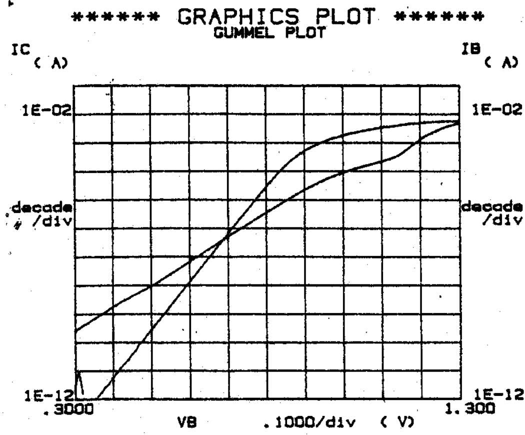


Figure 11. Gummel plot of NPN transistor with modified trench.

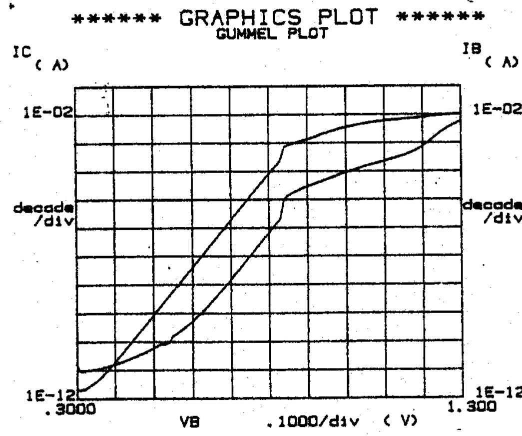


Figure 12. Gummel plot of NPN transistor with increased emitter to trench spacing

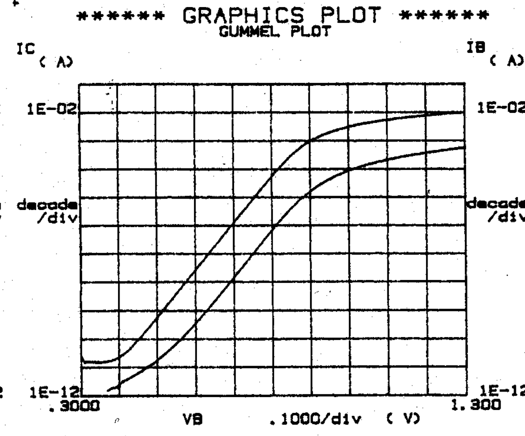
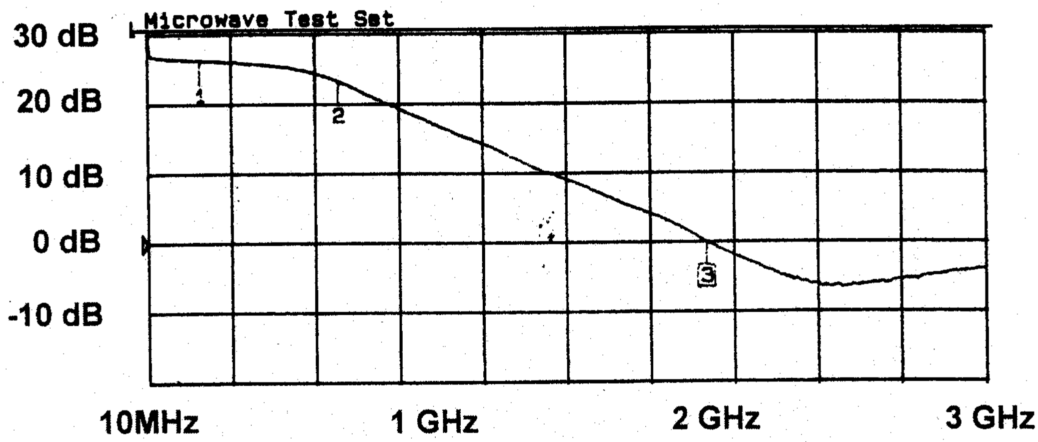


Figure 13. Gummel plot of guarded NPN transistor.



Marker	Frequency	Gain
1	197 MHz	26.2 dB
2	690 MHz	23.2 dB
	900 MHz	18 dB

Figure 14. Gain plot of low power R.F. amplifier.

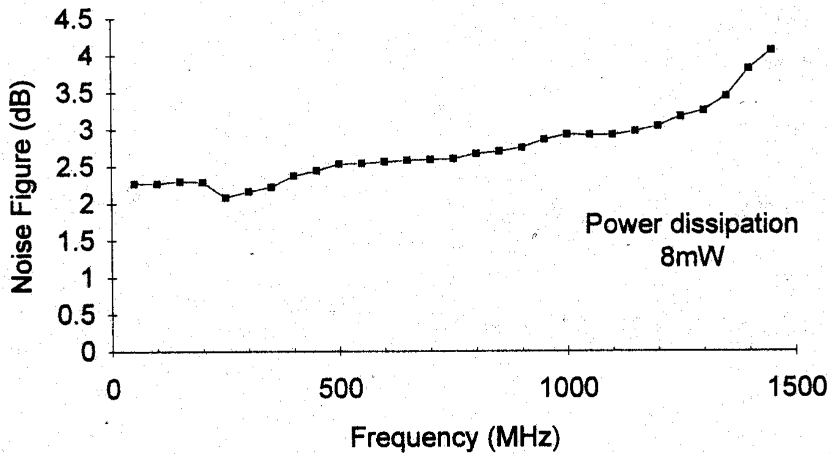


Figure 15. Noise Figure plot for low power R.F. amplifier.