

## HVIC Process on Bonded Wafers with Internal Gettering

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### Abstract

A high voltage BiCDMOS process, using bonded and trench isolated wafers, was developed for internal use and foundry opportunities. Extensive use was made of the oxide isolation to achieve electrical isolation of >1000V between elements. The Oxide isolation also allows high packing density, positive and negative voltages on the same chip, noise reduction and allows devices which inject minority carriers into the substrate. This process supports a rugged, vertical 350V DMOS, 10V CMOS, vertical NPN, lateral PNP, and a 450V SCR, together with a variety of components such as resistors, high and low voltage capacitors, Zener diodes, etc. We propose for the first time, the use of internal gettering in combination with high temperature denuding of the active layer using thermal oxidation techniques to achieve high minority carrier lifetime and enhanced gate oxide integrity (GOI). The internal gettering was achieved by the use of a pre-bond implantation and resulted in significantly enhanced minority carrier lifetime of the SOI layer.

### Introduction

High voltage IC's have wide applications in telecommunications, off-line power, display and smart power. Achieving HVIC's using conventional technologies has resulted in specialized processes for unique applications. These frequently require off-chip components as well as placing several restrictions on the circuit designers. As a result, older, expensive technologies, such as V-groove DI or variations of this technology are still widely used for HVIC applications. Bonded and trench isolated technology allows a truly universal process to be developed, which can have a broad array of applications and still be cost competitive compared to DI or discrete/hybrid implementations. This cost advantage is achieved for two reasons, the ability to process larger diameter wafers, thus gaining manufacturing efficiency, and the vertical trench isolation, gaining area efficiency. Depending on the applications, utilizing bonded and trench isolated material can double the number of chips per wafer. This "state of the art" process

technology demonstrates the advantages stated above.

### Process

The process begins with a device wafer, which has been selected to achieve a tight resistivity tolerance required for the various competing design requirements of the HVIC process. The vertical power DMOS device and the vertical NPN device require a low impedance path to the surface and as a result, the device wafers receive a heavy N+ implant prior to bonding (buried layer implant). (Fig 1) After bonding and thinning to the appropriate thickness, the wafers are trench isolated utilizing an aggressive vertical ICP etcher. This etch is very important to the fabrication of the starting material. It utilizes a one-step etch technique that stops on oxide with no undercutting<sup>1</sup>. (Fig 2) The sidewalls of the trench are then phosphorus doped to provide a low resistance vertical current path that attaches to the buried arsenic implant. After doping, the trenches are passivated and filled with a combination of oxide and polysilicon and then planarized using conventional CMP techniques.

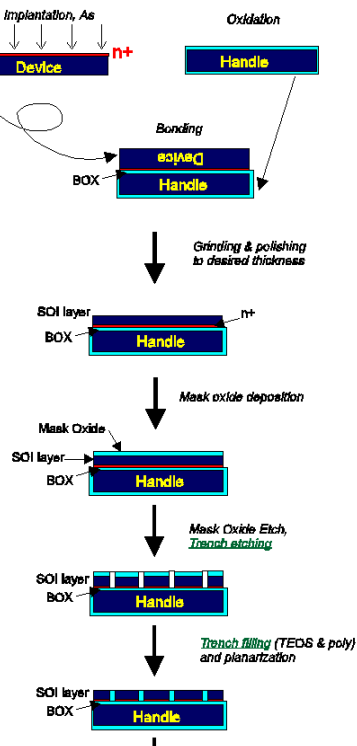


Figure 1. Bonded and Trench Isolated starting material process flow.

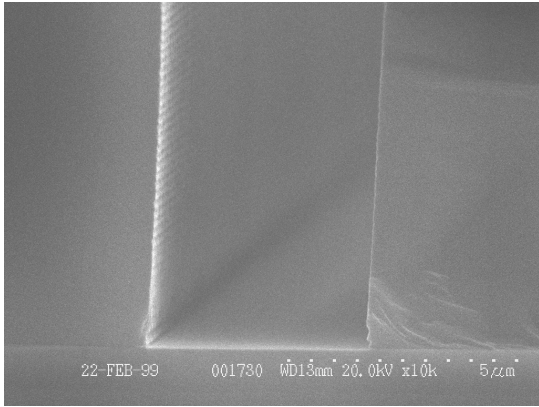


Figure 2a

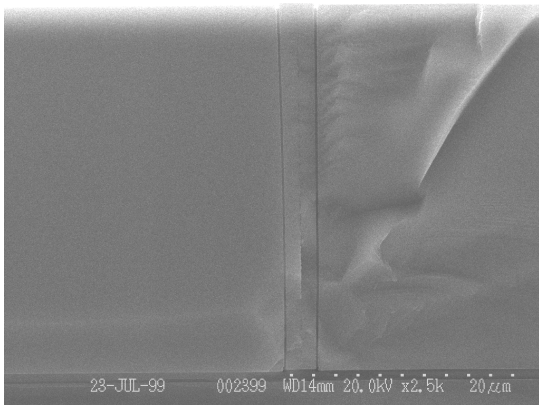
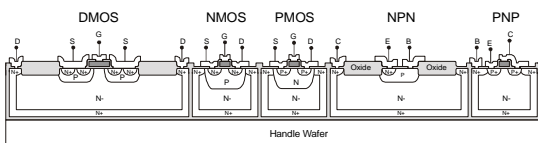


Figure 2b.

**SEM of ICP deep silicon etch, stop on oxide prior to fill. (2a). Trench etched SEM filled with liner oxide and polysilicon (2b).**

The devices are then fabricated on a LOCOS based BiCDMOS process designed for high voltage. This 12-mask process has a nominal two-micron field oxide, P-well self-aligned polysilicon gate CMOS and a DMOS transistor of novel design. This process supports a 350 V vertical DMOS transistor, a 150 V HVMOS device, 10V CMOS, a vertical NPN and lateral PNP, and a range of resistor sheet resistances. A cross-section and list of device characteristics of the BiCDMOS process (P10) is shown in Fig 3 and 4. All integrated components are isolated by >1000V.

**Cross-section of the BiCDMOS process**

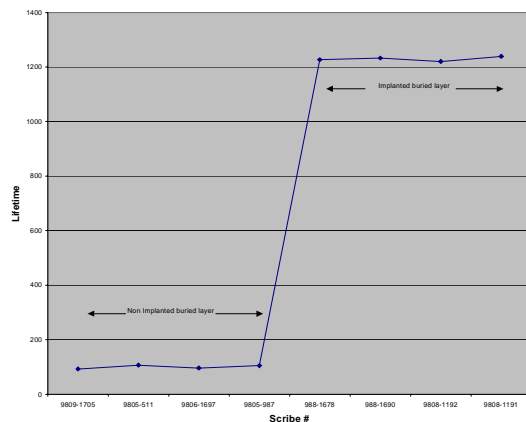


**Figure 3. A cross-sectional representation of the BiCDMOS process.**

<b><u>Device Characteristics</u></b>	
<b>DMOS</b>	$B_{vdss} > 350V$ , $R^*A = 50m\Omega\text{-cm}^2$
<b>CMOS</b>	$B_{Vdss} > 10\text{volts}$
<b>NPN (vertical)</b>	$B_{Vceo} > 50\text{ volts}$ , $\beta > 100$
<b>PNP (lateral)</b>	$B_{Vceo} > 20\text{ volts}$ , $\beta > 300$
<b>Resistors</b>	15, 50, 350, 600, 2400 $\Omega/\text{sq}$
<b>Capacitors</b>	$.07\text{fF}/\mu\text{m}^2 @ 1000\text{ volts}$ $-.98\text{fF}/\mu\text{m}^2 @ 20\text{ volts}$

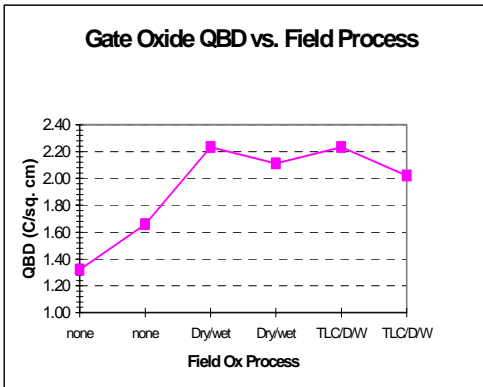
**Figure 4. BiCDMOS device Characteristics**

One of the most important reliability aspects of any MOS based process is Gate Oxide Integrity (GOI). As a result, the bonded SOI was extensively evaluated against bulk and epitaxial control wafers. To eliminate any influence from potential gettering by the phosphorus doped trench sidewalls; GOI testing has first evaluated on unpatterned SOI wafers. It was found that device wafers, which received an implantation prior to bonding, exhibited clearly superior GOI to wafers which received no implant. (Fig 5) To understand this effect we studied the minority carrier lifetime and the charge to breakdown of these implanted and non-implanted SOI wafers using the SCA (Surface Charge Analysis) technique. As seen in Fig 5, wafers that received the buried Arsenic implant prior to bonding exhibited a higher minority carrier lifetime than that of the non-implanted<sup>3</sup>. The data was also compared to bulk wafers and epi wafers. The buried layer implanted SOI and Epi wafers exhibited similar SCA results (high SCA lifetimes) whereas the results from bulk exhibited similar (Low SCA lifetimes) as the non-implanted SOI.



**Figure 5. SCA lifetime graph for 200nm wet oxidation.**

We can explain these results by looking at Internal Gettering and denuding technology. Internal gettering technology was found to be essential to achieve high yields in the fabrication of the BiCDMOS process on bonded and trench isolated starting materials. The buried layer implant tends to attract transition metals (Fe, Cu, etc.) that have contaminated the wafer in subsequent thermal processing steps. These contaminants become recombination centers and cause high junction leakage, gate oxide defects and nucleate dislocations<sup>2</sup>. This internal gettering in conjunction with the lowering of the oxygen content of the device layer by methods of high temperature denuding provide very reliable gate oxides for this BiCDMOS process.(Fig 6)



**Figure 6.** QBD analysis (charge to breakdown) of SOI with different Thermal oxide denuding steps. Note the increase in QBD as denuding of the active layer takes place

The buried implant also acts as a backside electrical contact for the vertical devices on this process. It acts as the drain region of the vertical DMOS devices and the collector of the vertical NPN devices. The buried layer is contacted through a sidewall diffusion of phosphorus that contacts the buried layer (wrap-around region) and brings it to the top of the silicon tub. This allows for topside drain and collector contacts. (Fig 7)

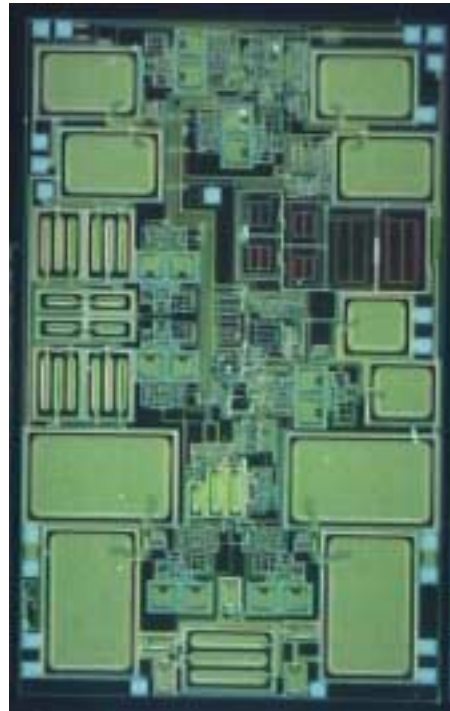
SOI starting material



**Figure 7.** Cross sectional representation of the Bonded and trenched starting material. Highlighting the wrap around-region.

### Conclusion

In conclusion, we are presenting a HVIC BiCDMOS process on a bonded and trench isolated wafer with enhanced gate oxide integrity as a result of internal gettering. This advanced 350V process has passed rigorous internal qualification and is in commercial production for both internal requirements and foundry opportunities (fig 8). Further we present, for the first time, a significant minority carrier enhancement as a result of pre-bond implantation processing.



**Figure 8.** Photo of Line Card Access product produced by CP Clare Corporation. This product utilizes the 350V BiCDMOS process.

### REFERENCES

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