Complementary Bipolar Fabricated by the Bonding of Patterned Buried Layers

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Complementary bipolar, the CMOS of bipolar, is an attractive technology for a number of high speed, high precision applications. These include AID converters, smart power and instrumentation circuitry. Conventional technology places severe limits on the fabrication of these devices because of the high diffusivity of the boron P+ buried layers, which wafer bonding can overcome. With pre-bond, device wafer processing, ideal complementary bipolar processes can be developed. This requires the bonding of patterned buried layers. In this paper we will examine the issues related to patterned wafer bonding and demonstrate a commercial high performance complementary bipolar process in which 6 masking steps are used on the device wafer prior to bonding to achieve a nominall00V complementary bipolar process.

Conventional buried layers are formed using epitaxial technology in which the buried layer pattern is photo defined on the base wafer and then the epi layer is grown on top. Epitaxial technology limits the peak doping concentration and the profile control of high diffusivity layers such as boron. This limits epi based complementary bipolar circuits to operating voltage of < I OV. Wafer bonding offers a number of potential improvements over epitaxial technology. The crystalline quality of the SOI layer is unaffected by the buried layer doping allowing an order of magnitude higher doping than with epitaxial technology. SOI technology does not suffer from autodoping and can put the buried layer in as the last high temperature step. As a result it is possible to achieve abrupt profile control on P+ buried layers. For this complementary bipolar process the high temperature steps of well and sinker diffusion are done before the P+

buried layer; this is impossible with epi. Simulations shows that this step reversal allows this high voltage complementary structures to achieve a rating of over 200V.

Patterned buried layers have a combination of heavily doped layers and surface topology, both of which maker bonding difficult. Figure I is a scanning acoustic microscope (SAM) image of a conventionally bonded wafer with a patterned buried layer showing periodic voiding associated with the pattern. In this case, the majority of the wafer is only lightly doped which bonded whereas the heavily implanted areas are voided. Grinding and polishing reveal perfect geometric voids defined by the implantation pattern. It is widely known that the implantation process causes a volume expansion in the surface of the wafer, which results in a step on the surface. This step is a function of implantation techniques and conditions and can range from 2-15nm depending on machine and specie. We developed a technique to reproducibly generate controllable step heights, which allowed the bonding to be characterized. We examined this step height directly after implant, after a low temperature recrystallization and after a high temperature anneal. Based on this analysis we developed a voidless bonding technique which will be discussed further in the talk.

The complementary bipolar process starts with a lightly doped device wafer into which an alignment mark is etched to allow
alignment of the topside pattern to the backside pattern. Then a P well is defined, implanted and driven deeply into the wafer to establish the P "epi" layers. Next N+ and P+ sinker regions are defined, implanted and driven to the depth of the final SOI layer. Final the N+ and P+ buried layers are defined and implanted. The wafers are then bonded to oxidized handle wafers and thinned using conventional grinding and polishing. These wafers bonded voidlessly using the optimized techniques. Fig 2 is one such wafer, which has been thinned by polishing to the bonded oxide. Because the polishing slurry is selective to P+ , it left the P+ sinker and buried layer remaining. The uniform color under the N+ areas and the remaining P+ show the high integrity of the bond. After SOl formation the wafer is trenched and refilled using oxide and polysilicon. The wafer was then process through a commercial foundry for the front

side bipolar processing. The performance of the resulting bipolar will be reviewed in the talk.

In summary, this paper presents the voidless bonding of extensively pre-processed device wafers with excellent bond and device circuit yield. This new technology opens many opportunities for future development.

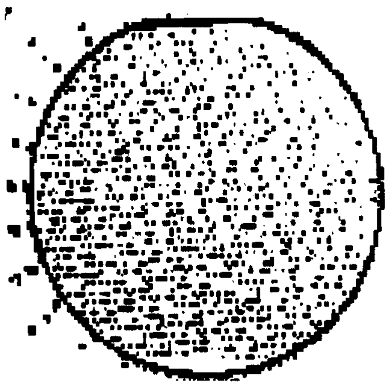

Fig 1

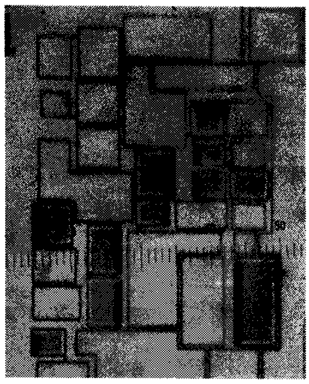

Fig 2