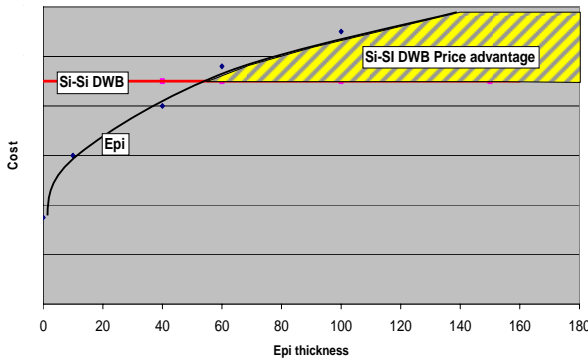


# Si-Si Direct Wafer Bonded Epi wafers

For semiconductor device manufacturers, silicon – silicon direct wafer bonding offers a cost effective alternative to conventional epitaxial layers for high voltage power devices such as MOSFETs, PIN diodes and IGBTs.

Cost of epitaxial layers on Silicon vs thickness of epi layer

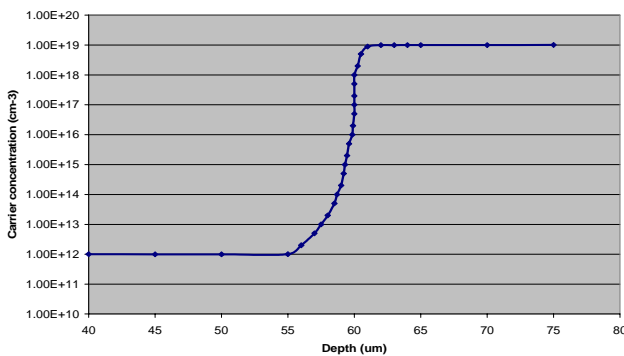


## Key Features

- High Quality
- Low cost
- Low defect density
- Excellent Layer uniformity
- Multiple layers
- Sharp transitions
- Layer resistivities up to 10kΩ-cm
- Excellent interface quality

The use of direct wafer bonding technology allows silicon substrates to be produced containing multiple layers of single crystal silicon. These layers can have resistivities ranging from 1mΩ-cm to 10kΩ-cm, n and p-type and can include combinations of orientations – a feature not possible with conventional epitaxy. The bonding process give a high quality wafer with low leakage, low warp and a low defect density. Additionally, the thickness variation in the layers can be as little as 0.5μm – even on 100μm thick layers. Also, the transition between high and low dopant levels can be sharp or soft, depending on the application or customer requirement.

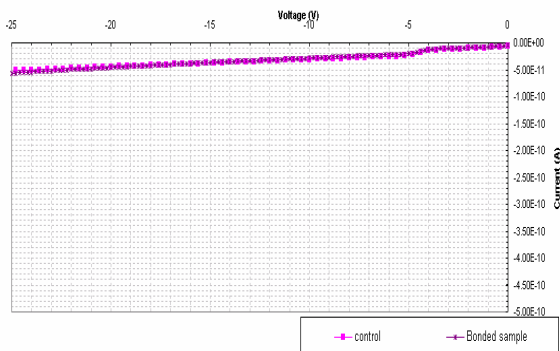
Dopant profile across bonded junction



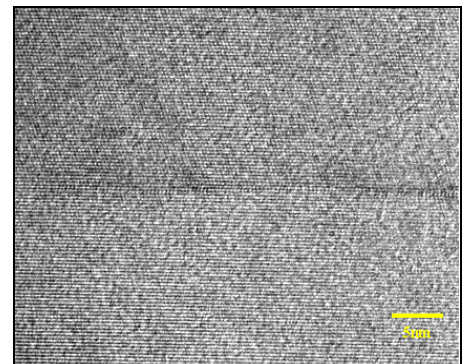
## Applications

- High voltage PIN diodes
- RF attenuators
- Photodetectors
- X-ray detectors
- IR sensors
- HV Power Devices
- Replacement for epitaxial deposition

Electrical testing indicates that there is no difference in leakage current from diodes made on bonded silicon compared with those made on standard bulk Si substrates and high resolution transmission electron microscopy has shown the bonded interface to be free of defects and stress

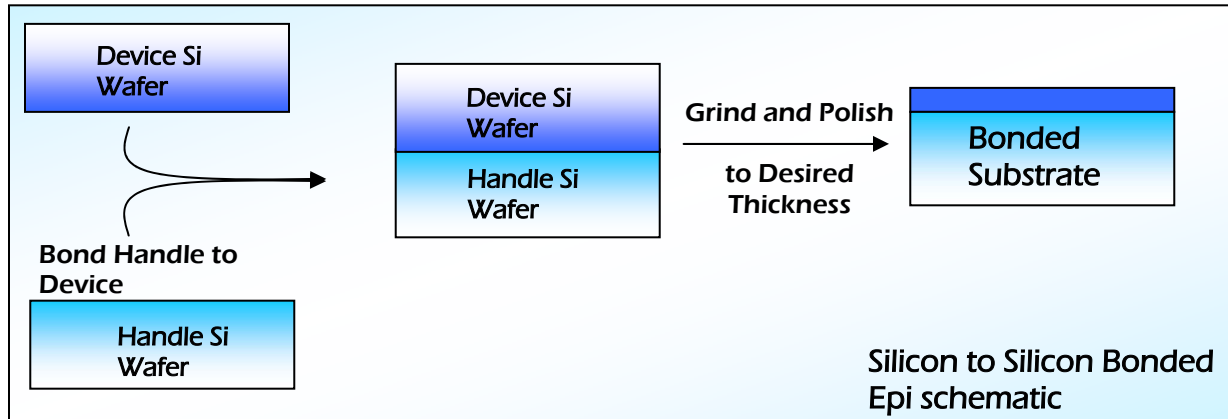


Comparison of diode leakage current on DWB and standard Silicon substrates



High Resolution TEM image of DWB wafer face

# Si-Si Direct Wafer Bonded Epi wafers



Parameter	Unit	Specification Range
Wafer Diameter	Mm	100, 125, 150
Handle Layer Specifications		
Handle Thickness	$\mu\text{m}$	350 – 700
Handle Thickness Tolerance	$\mu\text{m}$	+/- 5
Dopant Type		N or P
Doping		N-Type: Sb, As, P; P-Type: B
Resistivity	$\Omega\text{-cm}$	>0.007
Growth Method		CZ or FZ
Crystal Orientation		<100> or <111>
Backside Finish		Lapped/Etched or Polished
Device Layer Specifications		
Device Layer Thickness	$\mu\text{m}$	2 – 200
Tolerance	$\mu\text{m}$	+/- 0.5 or +/- 1
Dopant Type		N or P
Doping		N-Type: Sb, As, P; P-Type: B
Resistivity	$\Omega\text{-cm}$	>0.007
Growth Method		CZ or FZ
Crystal Orientation		<100> or <111>
Buried Layer Implant		N- Type of P-Type