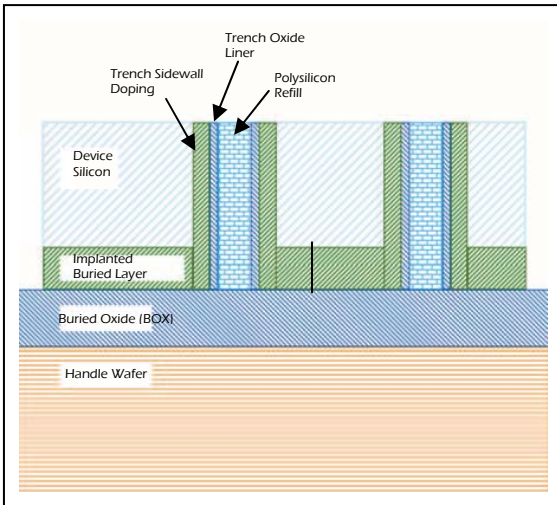
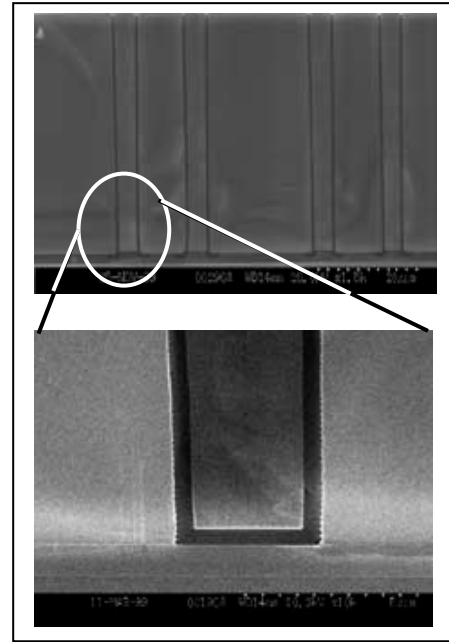


Dielectric Isolation IC Solutions



ICEMOS Technology presents its dielectric isolation technology –delivering perfect isolation between high voltage components on the same chip. Isolation is achieved using thick film SOI technology combined with state of the art high aspect ratio deep trench etching and oxide/poly refill. This technology is available on all wafer sizes from 100mm to 150mm and silicon device layers from 2um to 90um

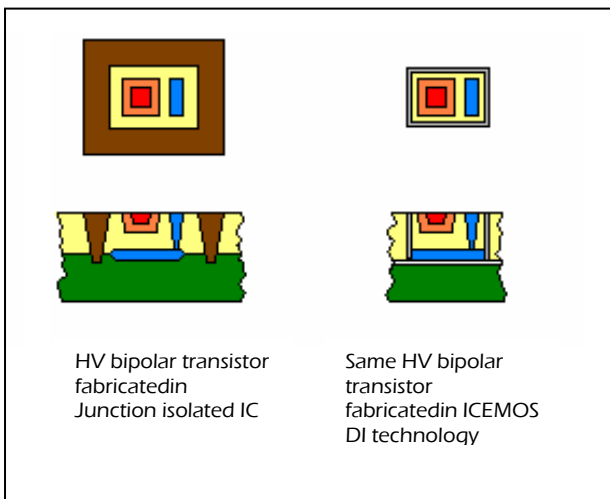
Dielectric Isolated Substrate Structure illustrating options available to designers



SEM Micrographs showing high aspect ratio trench isolation with oxide poly refill. Note – zero undercut of buried oxide layer at bottom of trench

Key Features

- Complete device isolation – up to 1000 Volts
- Allows significant die shrink compared with conventional Junction isolation
- Much lower defect density than conventional DI technologies
- Lower Substrate capacitance than bulk
- Lower cost than trench isolation on epi
- Technology scalable to 150mm and above



Comparison of HV bipolar IC transistors made on junction isolated and ICEMOS DI technologies, showing 3x saving in silicon real estate

Applications

- Solid State Relay photovoltaic generators
- Photovoltaic cells and Optoelectronic devices/ICs
- High Voltage analog ICs for telecommunications
- High performance bipolar circuits
- Smart Power ICs
- Integrated Sensors

Dielectric Isolation IC Solutions

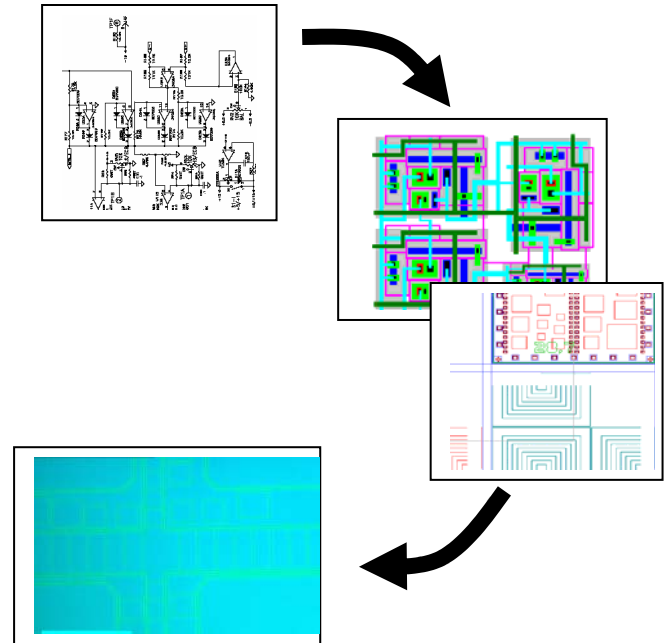


Supply Options Available

- Provision of DI Substrate from isolation mask provided
- Provision of Fully processed DI IC using ICEMOS as foundry to complete post isolation processing
- Provision of Full IC design and fabrication on DI from customer schematic

Post Isolation technologies available

- Simple Bipolar
- CMOS (1P, 2M)
- BiCMOS (1P, 2M)



Parameter	Unit	Specification Range
Wafer diameter	mm	100, 125, 150
Handle Layer Specifications		
Handle Thickness	μm	350 – 700
Handle Thickness Tolerance	μm	+/- 5
Doping		N-Type: P, As, Sb, or P-Type: B
Resistivity	Ω-cm	0.01 - 10000
Growth Method		CZ or FZ
Crystal Orientation		<100> or <111>
Backside finish		Lapped/etched or Polished
Buried Oxide Specifications		
Thermal oxide grown on		Handle, or, Device, or Both
BOX Thickness	μm	0.2 – 3.0
Device Layer Specifications		
Device Layer Thickness	μm	2 – 100
Tolerance	μm	+/- 0.5 or +/- 1.0
Doping		N-Type: P, As, Sb, or P-Type: B
Resistivity	Ω-cm	0.01 - 10000
Growth Method		CZ or FZ
Crystal Orientation		<100> or <111>
Buried Layer Implant		N-Type or P-Type up to $1e^{16}cm^{-2}$
Trench and Refill Specifications		
Trench Mask tone		Positive resist
Trench Mask type		E-beam master for projection aligner
Trench line width	μm	>2um
Trench Aspect ratio		10:1 standard. Up to 20:1 possible
Trench Sidewall doping type		N (Phosphorous)
Trench refill – oxide (each sidewall)	μm	0.1 – 1.0
Trench refill - polysilicon		To fill
Planarisation		CMP
Final field oxide	μm	Thermal oxide + TEOS up to 2.0 μm

